Hardware Specification

S-7601A
TCP/IP Network Stack LSI

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1 Introduction

1.1 Product Overview

The S-7601A is a LSI that integrates TCP/IP network stack. It offers your devices a quicker and easier connectivity to a network with its on-chip serial interface and a static RAM that operates as a buffer. Implementing this LSI into your system can significantly reduce your software development cost. Also its low operating frequency gives benefits to the power consumption.

The S-7601A also supports a microprocessor interface via the iReady iAPI™ register set, and connection to Physical Transport Layer Interface. iAPI consists of a set of register and operating definitions that allow any micro controller system to interface with the internal modules.

The S-7601A is an extension of the S-7600A. This product has the S-7600A-compatible mode at the register set level. Therefore, existing S-7600A software resources can be used effectively.

1.2 Features

- Industry standard protocols support :
  TCP/IP (Ver. 4.0)
  PPP (STD-51-compliant)
  UDP
- General purpose sockets :
  Configured for two sockets
- MPU interface :
  68k/x80(MOTO/Intel) bus interface
  or two-mode synchronous serial interface (SII serial and SPI)
- Physical Transport Layer Interface :
  Universal Asynchronous Receiver/Transmitter (UART)
- Low clock rate :
  Multiplied four by the bit-rate
- Operating frequency :
  256kHz typical
- Low power consumption :

Full-transmitting Operating current consumption :	0.9	mA	typ.
Non-transmitting Operating current consumption :	160	µA	typ.
Standby current consumption :	1.0	µA	typ.

- Stand-by mode :
  held by RESET signal
- Wide operating voltage range :
  2.4V to 3.6V
- Easier application development :
  portable iAPI™ support

1.3 Extension of the S-7600A

- Function extension
  Automatic IP assignment
  CHAP support function
- Performance extension
  Round Trip Timer (RTT)
  Increase in the buffer size
- Delayed ACK

1.4 Differences with S-7600A

- Two-mode register map
  The New_Reg bit in the general control register (0x01) is used for selection.
  The default is the S-7600A-compatible register map.
- An SPI serial interface is added to the MPU interface.
  SPI is selected by pulling the PSX pin low and the C86 pin high.
- Improvements of MPU interface timing
  Busy signal output timing
  Address/data hold time
  Enable/control pulse width
- The NC pin (#38) is used as a test output pin so that #38 must leave OPEN.

1.5 Trademarks

1.6 Definitions

- IP Internet Protocol
- PPP Point-to-Point Protocol
- TCP Transmission Control Protocol
- UDP User Datagram Protocol
- API Application Programming Interface

1.7 Cautions

1. DO NOT apply a voltage or current that exceeds the absolute maximum ratings to terminals. If applied, the IC may malfunction or be destroyed.
   The standard values are set with sufficient margins, but use the IC within the recommended operating conditions to optimize device quality.
2. Measures against static electricity
   When transporting or storing ICs, use conductive containers or metal coated boxes.
   Check that there is no current leakage in electrical facilities, and be sure to ground them.
   Also ensure that workbenches and people who handle ICs are grounded.
3. Excessive external noise to the power supply or I/O terminals of CMOS ICs causes latch-up, leading to faults and damage. If latch-up has occurred, immediately turn off the device, eliminate the cause, and turn on the device again.
4. Keep the IC away from mechanical vibration, shock, and sudden changes in temperature. These may cause wires to break.
5. Environment
   5.1 Use and store ICs below the absolute maximum rated temperature.
   5.2 DO NOT use or store ICs where condensation can occur.
   5.3 DO NOT use ICs where they are directly exposed to dust, salt, or acid gas such as SO_2. These may cause leaks between element leads and cause corrosion.
   5.4 To store ICs for a long time, DO NOT process them. During storage, DO NOT apply any load to ICs.

2 Functional Block Diagram

Figure 2-1 shows a functional block diagram of the S-7601A. There are blocks of the Network Stack and other functions related to it. The S-7601A has the interface for a host MPU and a Physical layer for various data terminal equipment.

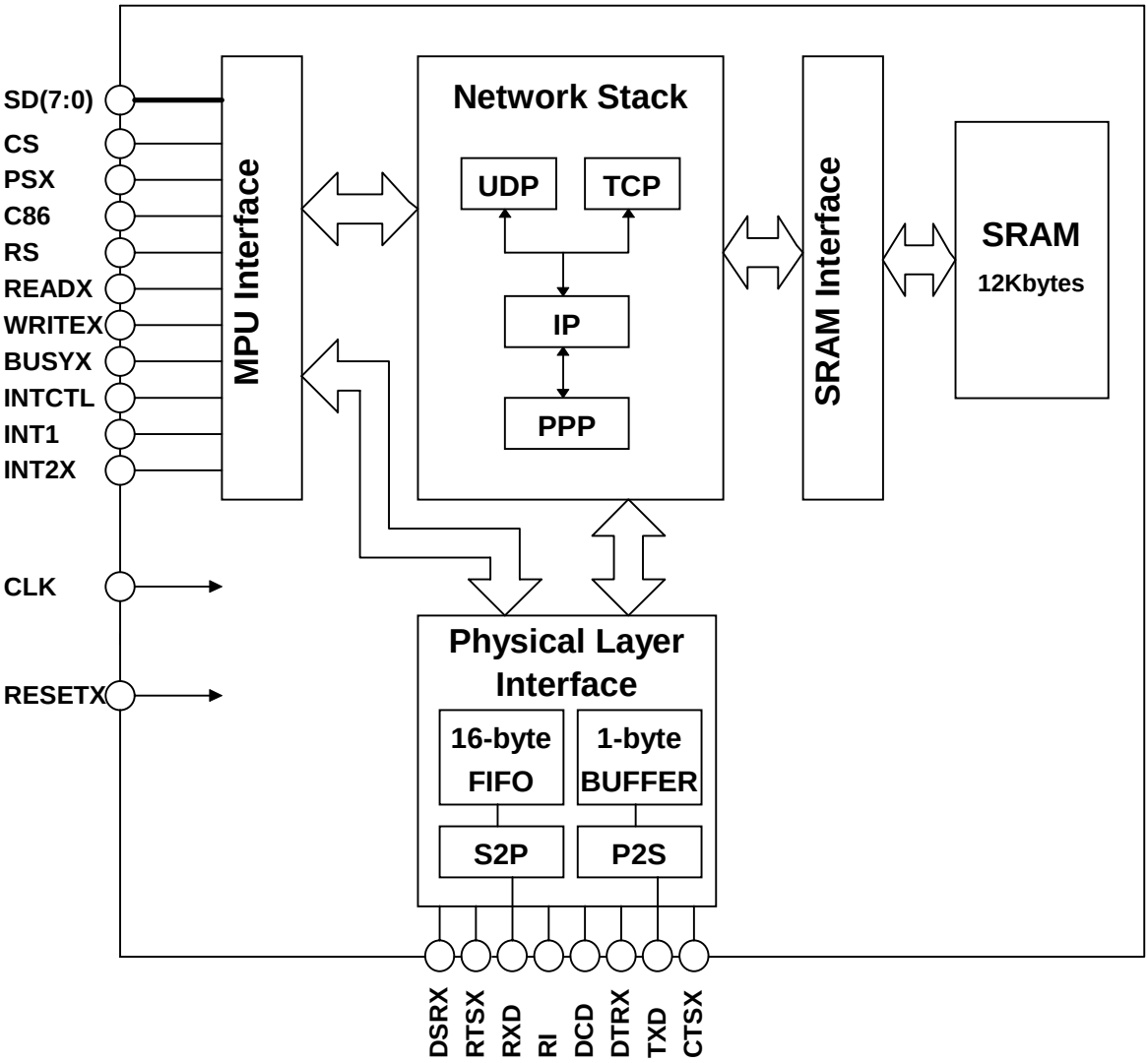


Figure 2-1 Block Diagram

The transport and network layers contain:

- Two general sockets that provide connectivity between the application layer and the transport layer.
- TCP/UDP module that allows for reliable (retransmission) and unreliable (no retransmission) datagram deliveries.
- IP module that provides connectionless packet delivery.
- PPP module that provides point-to-point connection link between two hosts.

3 Terminals

3.1 Pin Assignment

Figure 3-1 shows Pin Assignment in Package.
Table 3-1 shows signal names, listed by Pin Number.

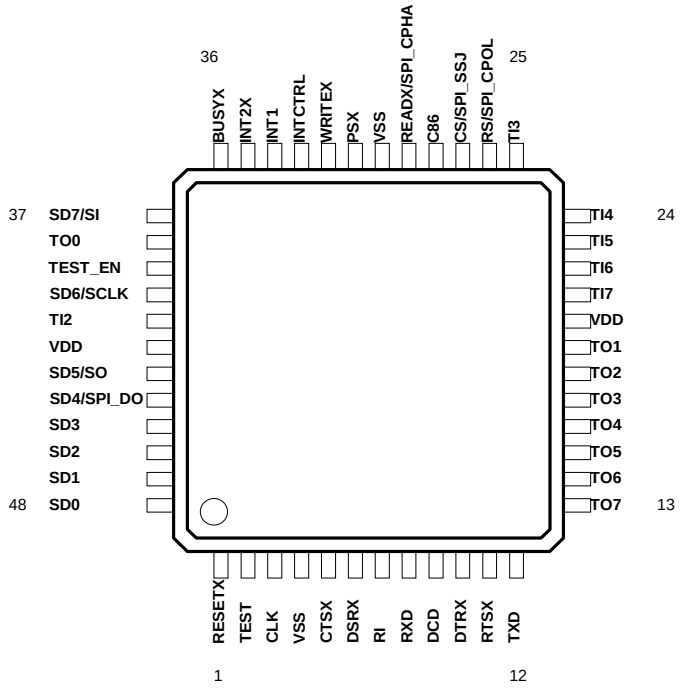


Figure 3-1 Pin Assignment

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	RESETX	13	TO7	25	TI3	37	SD7/SI
2	TEST	14	TO6	26	RS/ SPI_CPOL	38	TO0
3	CLK	15	TO5	27	CS/ SPI_SSJ	39	TEST_EN
4	VSS	16	TO4	28	C86	40	SD6/SCLK
5	CTSX	17	TO3	29	READX/ SPI_CPHA	41	TI2
6	DSRX	18	TO2	30	VSS	42	VDD
7	RI	19	TO1	31	PSX	43	SD5/SO
8	RXD	20	VDD	32	WRITEX	44	SD4/SPI DO
9	DCD	21	TI7	33	INTCTRL	45	SD3
10	DTRX	22	TI6	34	INT1	46	SD2
11	RTSX	23	TI5	35	INT2X	47	SD1
12	TXD	24	TI4	36	BUSYX	48	SD0

Table 3-1 Pin Assignment

3.2 Package Dimensions

S-7601A is housed in a 48-pin QFP package with 0.5mm pin pitch spacing. The package layout is depicted in Figure 3-2.

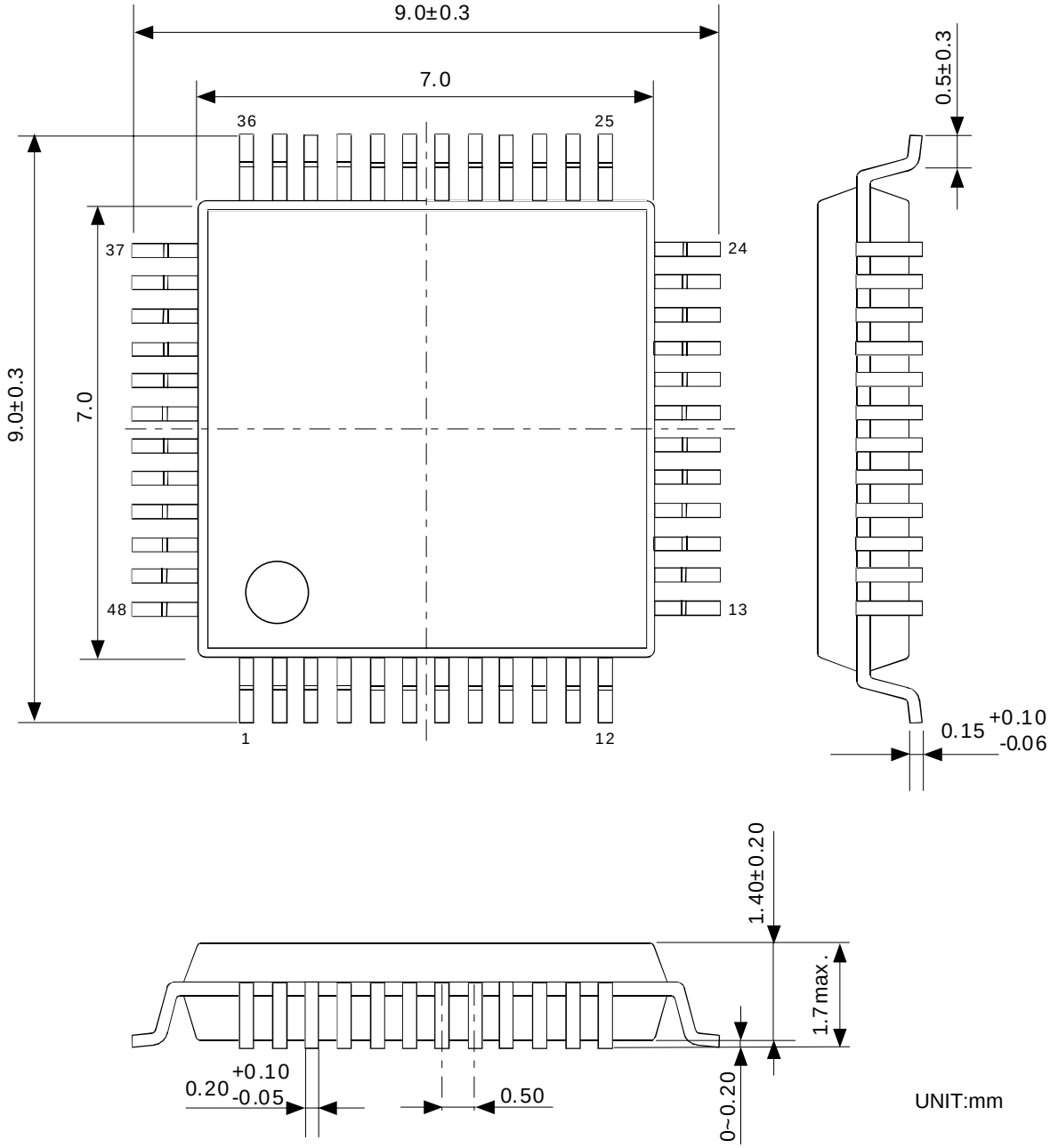


Figure 3-2 Package Dimensions

3.3 Pin Description

The pins and signal descriptions are listed by function in Table 3-2.

Name	I/O	Description	Type
VDD1,VDD2	-	Positive power supply	
VSS1,VSS2	-	GND potential	
RESETX	I	Reset input	A
TEST,TEST_EN TI2 to TI7	I	Test input (pull-down resistor is built in) When normal use, connect to Vss or open	B
TO0	*OT	Test output When normal use, open	E
TO1 to TO7	O	Test output When normal use, open	D
CLK	I	Clock input	C
CTSX	I	Clear to send input	C
DSRX	I	Data set ready input	C
RI	I	Ring indicator input	C
RXD	I	Serial received data input	C
DCD	I	Data carrier detect input	C
DTRX	O	Data terminal ready output	D
RTSX	O	Request to send output	D
TXD	O	Serial transmit data output	D
RS/SPI_CPOL	I	Register selection input/SPI CPOL input	C
CS/SPI_SSJ	I	Chip selection input/SPI Slave Select input	C
C86	I	MPU interface mode selection input 68k mode: 1 x80 mode: 0 SPI mode: 1 SII serial mode: 0	C
READX/SPI_CPHA	I	x80 mode: read requirement input 68k mode: enable input SPI mode: SPI CPHA input	C
PSX	I	Parallel/serial interface selection input	C
WRITEX	I	x80 mode: write requirement input 68k mode: read/write selection input SII serial mode: read/write selection input	C
INTCTRL	I	INT1/INT2X drive type (CMOS/OD) selection input	C
INT1	*OT	Interrupt output (active High) from S-7601A chip to MPU	E
INT2X	*OT	Interrupt output (active Low) from S-7601A chip to MPU	E
BUSYX	O	Busy indicator output	D
SD7/SI	*B	x80/68 mode: data bus SII/SPI serial mode: serial data input	F
SD6/SCLK	*B	x80/68k mode: data bus SII/SPI serial mode: serial clock input	F
SD5/SO	*B	x80/68k mode: data bus SII/SPI serial mode: serial data output	F
SD4/SPI_DO	*B	x80/68k mode: data bus SPI mode: SPI Data Order	F
SD0 to SD3	*B	Data bus	F

*OT : Tri-state output
*B : bi-directional

Table 3-2 Pin Description

3.4 Pin Configuration

Figure 3-3 shows configuration of each pin.

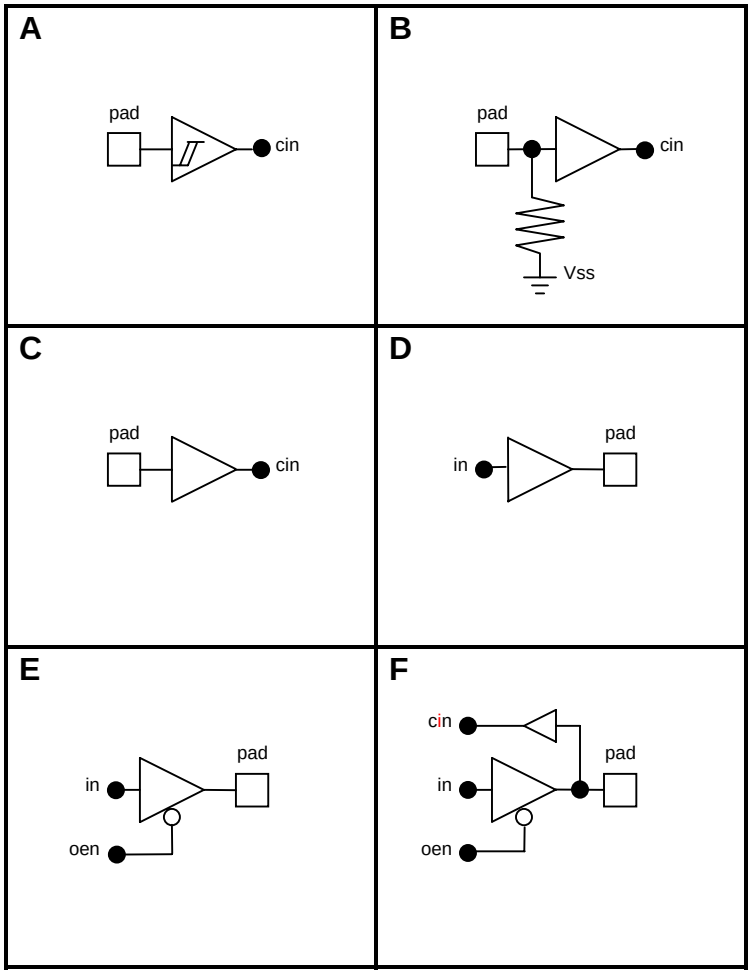


Figure 3-3 Configuration of Each Pin

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Parameter	Symbol	Conditions	Rating	Unit
Storage temperature	T_{sta}		-40 to +125	°C
Operating temperature	T_{opr}		-40 to +85	°C
Power supply voltage	V_{DD}	Ta=25°C	-0.3 to +4.0	V
Input voltage	V_{IN}	Ta=25°C	V_{SS}-0.3 ~ 5.5	V
Output voltage	V_{OUT}	Ta=25°C	V_{SS} to V_{DD}	V

Table 4-1 Absolute Maximum Ratings

4.2 Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
Operating Frequency range	F_{OPR}	Ta=-40 ~ +85°C	-	0.256	8	MHz	1
Clock Pulse width	Pw	Ta=-40 ~ +85°C	60	-	-	nS	
Operating voltage range	V_{DD}	Ta=-40 ~ +85°C	2.4	-	3.6	V	
Input voltage	V_{IN}	Ta=-40 ~ +85°C	0	-	5.0	V	

Note1: The clock is given by the CLK pin and needs to be as four times or more fast as the BIT rate.
(The multiplier is an integer whose tolerance is <±2%)

Table 4-2 Recommended Operating Conditions

4.3 DC Characteristics

Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, Ta=25°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Low level input voltage	V_{IL}		-	-	0.2× V_{DD}	V
High level input voltage	V_{IH}		0.8× V_{DD}	-	-	V
Low level input leakage current	I_{LL}	V_{IN}=V_{SS}	-1.0	-	1.0	µA
High level input leakage current	I_{LH}	All input terminals without pull-down resister V_{IN}=5.0V	-1.0	-	1.0	µA
High level input current	I_{IH}	All input terminals with pull-down resister V_{IN}=V_{DD}	18	70	220	µA
Low level output current	I_{OL}	V_{OL}=0.4V	5.0	-	-	mA
High level output current	I_{OH}	V_{OH}=2.6V	-	-	-3.5	mA
Schmitt Hysteresis voltage	V_{WD}		-	0.46	-	V

Table 4-3 DC Characteristics

4.4 Power Current Consumption

Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, Ta=25°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Full-transmitting Operating current consumption	I_{DD1}	Ta＝-40～+85°C F_{OPR}＝256KHz	-	0.9	2.2	mA
Non-transmitting Operating current consumption	I_{DD2}	Ta＝-40～+85°C F_{OPR}＝256KHz RESETX＝V_{SS}	-	160	320	µA
Standby current consumption	Is	Ta＝-40～+85°C	-	1.0	40.0	µA

Table 4-4 Power Current Consumption

5 MPU Interface

5.1 Overview

The S-7601A supports four MPU interfaces: two parallel modes and two serial modes. In parallel interface mode, the S-7601A can interface with x80 Family MPU or 68k Family MPU. In serial interface mode, the SII serial and the SPI serial are provided like the S-7600A. Table 5-1 lists an interface selection.

PSX	C86	Interface
0	0	SII Serial
0	1	SPI Serial
1	0	x80 Parallel
1	1	68K Parallel

Table 5-1 Interface Selection

5.2 Parallel Interface

Setting **PSX** to "H" select the parallel interface. In parallel interface mode the S-7601A can interface with either x80 Family MPU or 68k Family MPU. The desired MPU mode can be selected by setting the C86 pin to "H" or "L".

RS	68k Family MPU	x80 Family MPU		Function
	R/WX	READX	WRITEX	
1	1	0	1	Read Register
1	0	1	0	Write Register
0	1	0	1	Read Address Register
0	0	1	0	Write Address Register

Table 5-2 Connection Relationship between MPU and Pins

5.2.1 68k Family MPU Mode

This mode can be selected by pulling the **C86** input pin “H” and the **PSX** input pin “H”. In this mode, the address and data are muxed into a single 8-bit bus. All cycles start by placing an address on the bus and setting the **RS** pin to “L”. In this mode **WRITEX** signal works as read/write(R/WX) signal and **READX** is the enable(E) signal for 68k Family MPU interface. After the address cycle, the MPU generates a read or writes strobe by setting the **READX** and **WRITEX** pins. The S-7601A MPU interface logic assert a **BUSYX** signal low during data write and read phases. The MPU samples the **BUSYX** signal before starting a new cycle. The MPU can initiate a new cycle if the bit is “H”.

5.2.1.1 Write Cycle Timing

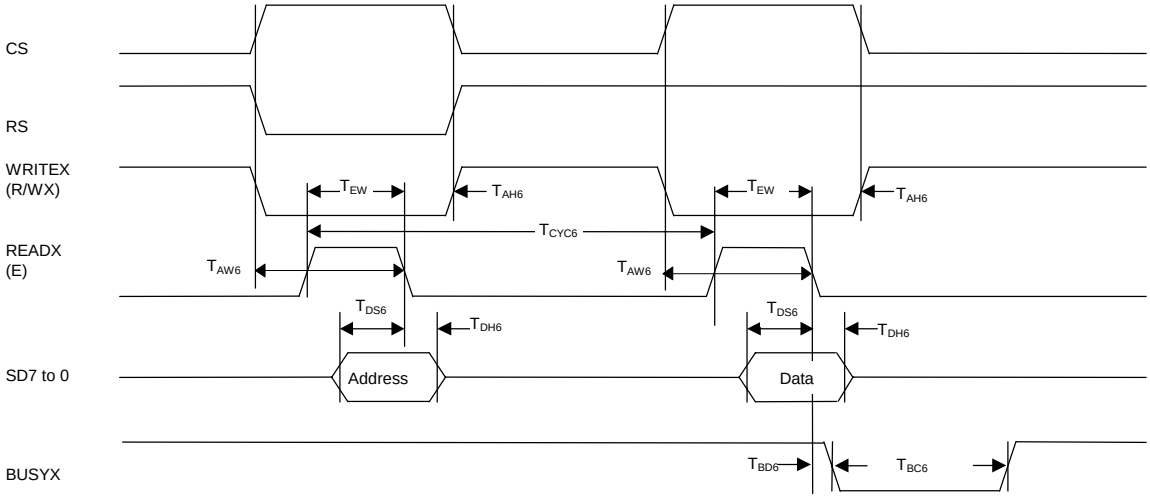


Figure 5-1 68k Family MPU Write Timing

Symbol	Description	Min	Max	Notes
T_{CYC6}	System Cycle Time	100 ns	-	
T_{AH6}	Address Hold Time	0 ns	-	
T_{AW6}	Address Setup Time	20 ns	-	
T_{DS6}	Data Setup Time	20 ns	-	
T_{DH6}	Data Hold Time	0 ns	-	
T_{EW}	Enable Pulse Width	40 ns	-	
T_{BD6}	BUSYX Delay Time	-	30ns	CL=80pF
T_{BC6}	BUSYX Pulse Width	2CLK	-	

NOTES:
- CLK is the clock of S-7601A
- Timing is specified of 50% of the signal waveform.
- Rise/fall time(20%,80%) of the input signal is 15nsec or less.

Table 5-3 68k Family MPU Write Cycle Timing

5.2.1.2 Read Cycle Timing

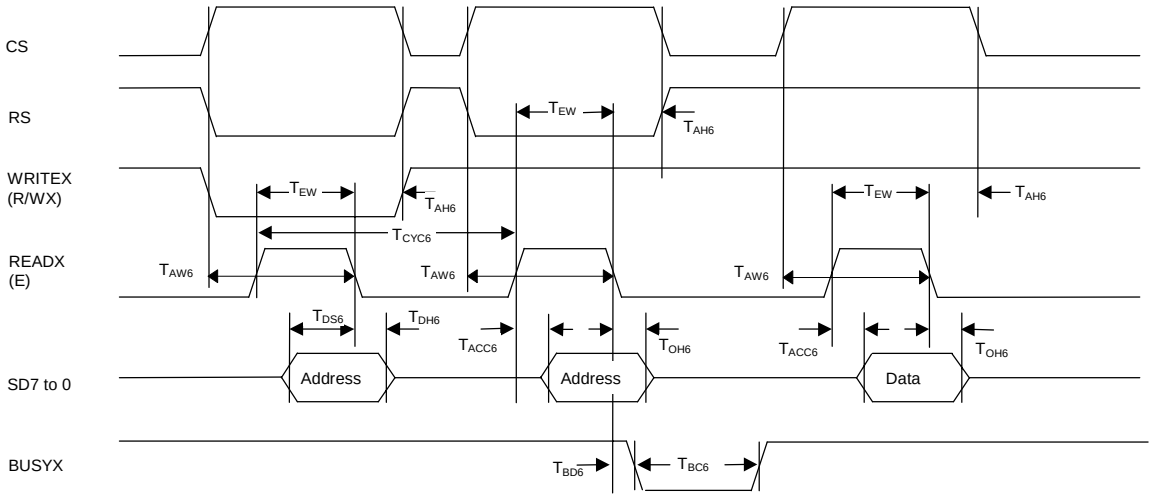


Figure 5-2 68k Family MPU Read Timing

Symbol	Description	Min	Max	Notes
T_{CYC6}	System Cycle Time	100ns	-	
T_{AH6}	Address Hold Time	0ns	-	
T_{AW6}	Address Setup Time	20ns	-	
T_{DS6}	Data Setup Time	20ns	-	
T_{DH6}	Data Hold Time	0ns	-	
T_{ACC6}	Access Time	-	30ns	CL＝80pF
T_{OH6}	Output Disable Time	20ns	-	CL＝80pF
T_{EW}	Enable Pulse Width	40ns	-	
T_{BD6}	BUSYX Delay Time	-	30ns	CL＝80pF
T_{BC6}	BUSYX Pulse Width	2CLK	-	

NOTES: • CLK is the clock of S-7601A
• Timing is specified of 50% of the signal waveform.
• Rise/fall time(20%,80%) of the input signal is 15nsec or less.

Table 5-4 68k Family MPU Read Cycle Timing

5.2.2 x80 Family MPU Mode

This mode is selected by pulling the **C86** input pin "L" and the **PSX** input pin "H". In this mode, the address and data are muxed onto a single 8-bit bus. All cycles start with the address placed on the bus. This address is then latched internally on the rising edge of **WRITEX**. The **RS** pin "L" indicates that the **WRITEX** strobe is for the address phase. In the next phase, data is either written or read by generating **WRITEX** or **READX** strobe. The MPU interface logic will assert the **BUSYX** signal after **READX** or **WRITEX** strobes are de-asserted. The **BUSYX** signal is de-asserted after the S-7601A complete a read or writes operation. The MPU samples the **BUSYX** signal before starting a new cycle. The MPU can initiate a new cycle after the **BUSYX** signal gets de-asserted.

5.2.2.1 Write Cycle Timing

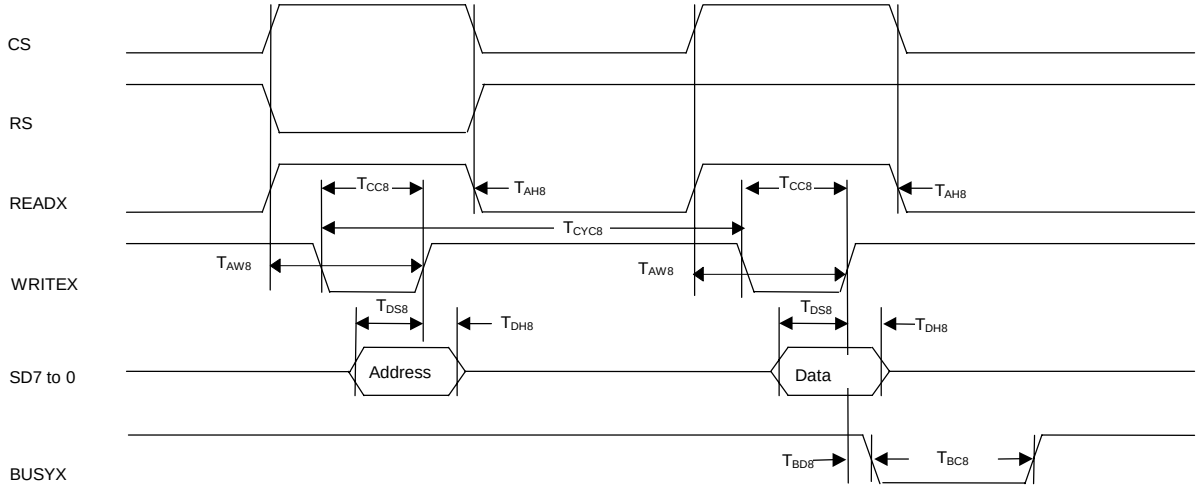


Figure 5-3 x80 Family MPU Write Cycle Timing

Symbol	Description	Min	Max	Notes
T_{CYC8}	System Cycle Time	100 ns	-	
T_{AH8}	Address Hold Time	0ns	-	
T_{AW8}	Address Setup Time	20ns	-	
T_{DS8}	Data Setup Time	20ns	-	
T_{DH8}	Data Hold Time	0 ns	-	
T_{CC8}	Control Pulse Width	40 ns	-	
T_{BD8}	BUSYX Delay Time	-	30ns	CL=80pF
T_{BC8}	BUSYX Pulse Width	2CLK	-	

NOTES:
- CLK is the clock of S-7601A
- Timing is specified of 50% of the signal waveform.
- Rise/fall time(20%,80%) of the input signal is 15nsec or less.

Table 5-5 x80 Family MPU Write Cycle Timing

5.2.2.2 Read Cycle Timing

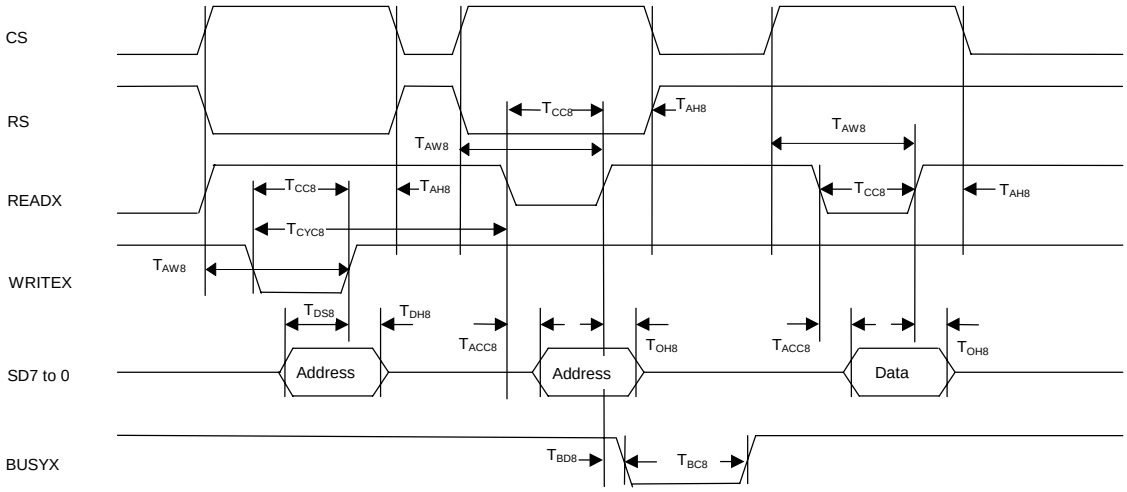


Figure 5-4 x80 Family MPU Read Cycle Timing

Symbol	Description	Min	Max	Notes
T_{CYC8}	System Cycle Time	100 ns	-	
T_{AH8}	Address Hold Time	0ns	-	
T_{AW8}	Address Setup Time	20ns	-	
T_{DS8}	Data Setup Time	20ns	-	
T_{DH8}	Data Hold Time	0 ns	-	
T_{ACC8}	Access Time	-	30ns	CL=80pF
T_{OH8}	Output Disable Time	20 ns	-	CL=80pF
T_{CC8}	Control Pulse Width	40 ns	-	
T_{BD8}	BUSYX Delay Time	-	30ns	CL=80pF
T_{BC8}	BUSYX Pulse Width	2CLK	-	

NOTES:
- CLK is the clock of S-7601A
- Timing is specified of 50% of the signal waveform.
- Rise/fall time(20%,80%) of the input signal is 15nsec or less.

Table 5-6 x80 Family MPU Read Cycle Timing

5.3 Serial Interface

This mode is selected by pulling the PSX input pin "L." In the mode, the SII serial and the SPI serial can be selected like the S-7600A. The SII serial can be selected by pulling the C86 input pin "L." The SPI serial can be selected by pulling the C86 input pin "H."

5.3.1 SII Serial Interface

This mode is selected by pulling the **PSX** input pin “L”. In this mode Bit 6 of the Data Bus is used as the serial clock and bit 5 and 7 are used as Data Output and Data Input. Bit 0 to 4 are high impedance. By pulling **WRITEX** signal to “H” or “L”, the MPU performs a read or write operation.

5.3.1.1 Write Cycle Timing

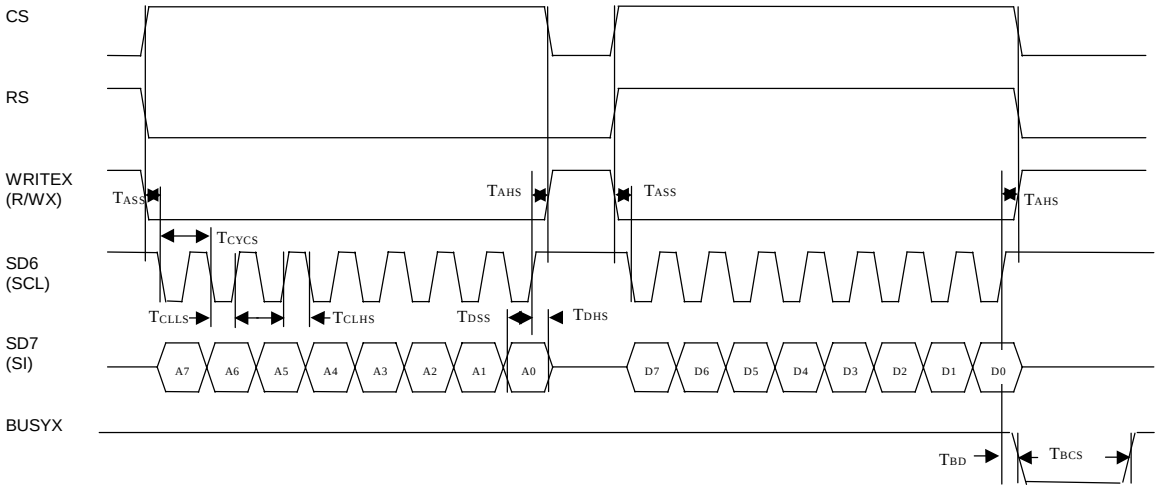


Figure 5-5 Serial Interface Write Timing

Symbol	Description	Min	Max	Notes
T_{CYCS}	System Cycle Time	100 ns	-	
T_{CLLS}	Clock L Time	40ns	-	
T_{CLHS}	Clock H Time	40 ns	-	
T_{ASS}	Address Setup Time	20ns	-	
T_{AHS}	Address Hold Time	20ns	-	
T_{DSS}	Data Setup Time	20ns	-	
T_{DHS}	Data Hold Time	20 ns	-	
T_{BDS}	BUSYX Delay Time	-	30ns	CL=80pF
T_{BCS}	BUSYX Pulse Width	2CLK	-	

NOTES:
- CLK is the clock of S-7601A
- Timing is specified of 50% of the signal waveform.
- Rise/fall time(20%,80%) of the input signal is 15nsec or less.

Table 5-7 Serial Interface Write Cycle Timing

5.3.1.2 Read Cycle Timing

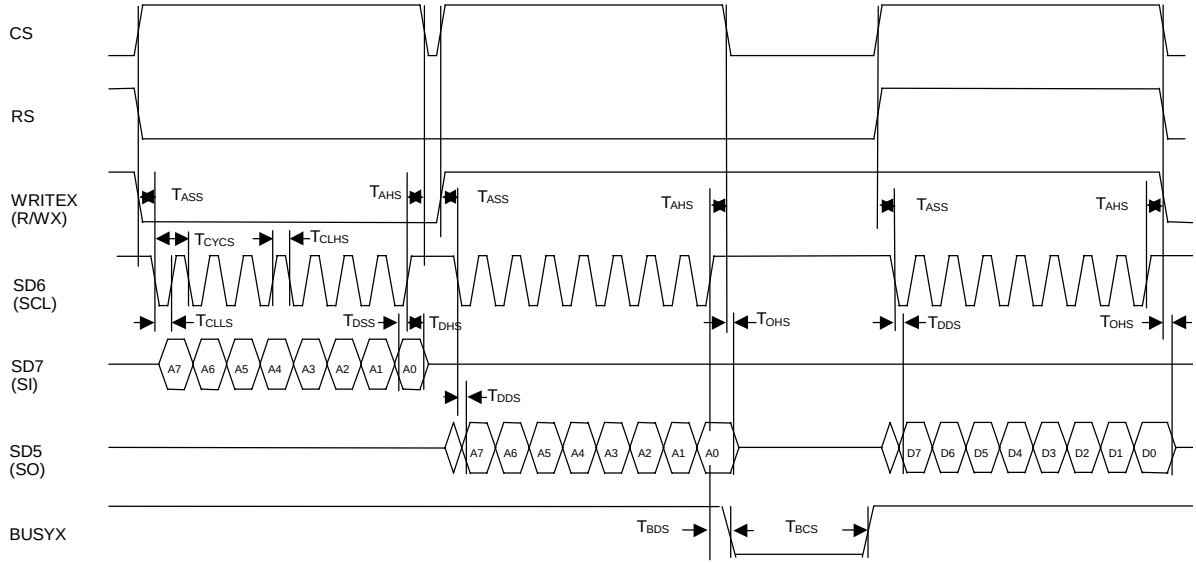


Figure 5-6 Serial Interface Read Timing

Symbol	Description	Min	Max	Notes
T_{CYCS}	System Cycle Time	100 ns	-	
T_{CLLS}	Clock L Time	40ns	-	
T_{CLHS}	Clock H Time	40 ns	-	
T_{ASS}	Address Setup Time	20ns	-	
T_{AHS}	Address Hold Time	20ns	-	
T_{DSS}	Data Setup Time	20ns	-	
T_{DHS}	Data Hold Time	20 ns	-	
T_{DDS}	Data Delay Time	-	30ns	CL=80pF
T_{OHS}	Output Disable Time	-	20ns	CL=80pF
T_{BDS}	BUSYX Delay Time	-	30ns	CL=80pF
T_{BCS}	BUSYX Pulse Width	2CLK	-	

NOTES:
- CLK is the clock of S-7601A
- Timing is specified of 50% of the signal waveform.
- Rise/fall time(20%,80%) of the input signal is 15nsec or less.

Table 5-8 Serial Interface Read Cycle Timing

5.3.2 SPI Serial Interface

5.3.2.1 Overview

The SPI (Serial Peripheral Interface) is a high-speed 3 wire serial bus common in many 8 bit CPU's and peripherals targeted at the 8-bit market. It is selected by setting he PSX input pin low, and the C86 input pin high.

In this mode, SD[6] is used as a serial clock (SCK), SD[7] is used as a serial input data pin (MOSI), SD[5] is used as a serial output data pin (MISO), and the CS pin is used as a slave select (SSJ). SPI devices are either masters or slaves. Master devices always provide the clock. The clock can be anywhere from near DC to 4Mhz. The S-7601A will always functions as an SPI slave device. For proper operations, the core clock frequency must be greater then 2x the SCK frequency.

MOSI stands for Master Out / Slave In, and MISO stands for Master In / Slave Out, making it obvious which lines are connected on the bus.

5.3.2.2 SPI Clock Formats

Several formats of clock and bit formats are possible. Shown below are byte waveforms different clock polarities and phases. The clock polarity (cpol) is controlled via the RS input pin, the clock phase (cpha) is controlled via the READX pin, and the data order is controlled by the SD[4] pin (0 = msb first). The S-7601A supports all four clock formats with any bit ordering.

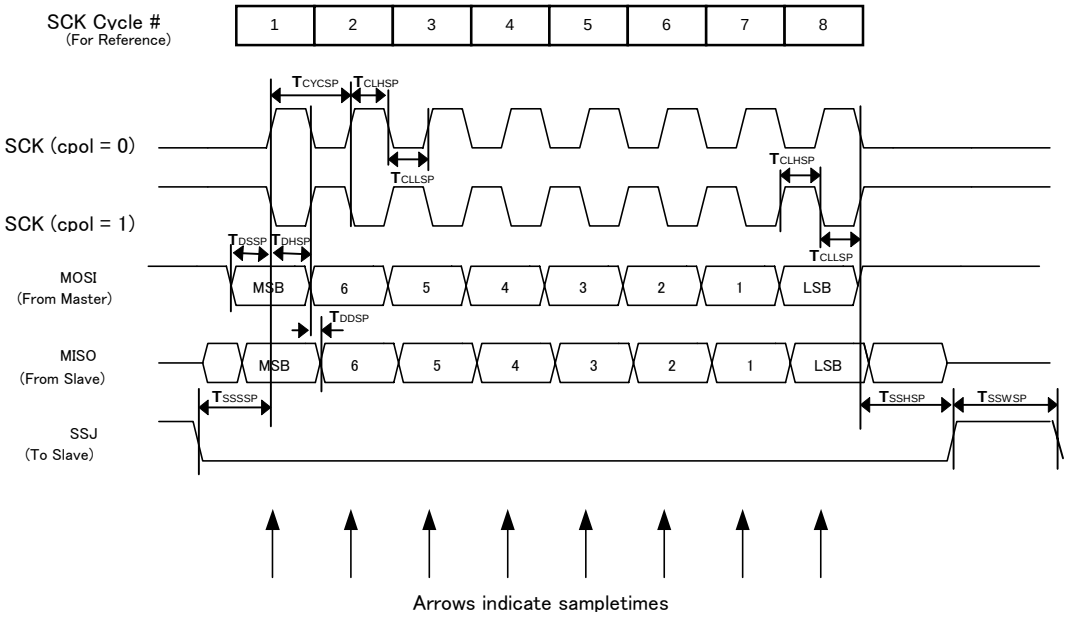


Figure 5-7 SPI Timing (cpha = 0, data order = 0)

Symbol	Description	Min	Max	Notes
T_{CYCSP}	System Cycle Time	250ns	-	
T_{CLLSP}	Clock L Time	40ns	-	
T_{CLHSP}	Clock H Time	40ns	-	
T_{DSSP}	Data Setup Time	20ns	-	
T_{DHSP}	Data Hold Time	20ns	-	
T_{DDSP}	Data Delay Time	-	30ns	CL=80pF
T_{SSSSP}	SSJ Setup Time	2CLK	-	
T_{SSHSP}	SSJ Hold Time	3CLK	-	
T_{SSWSP}	SSJ Disable Time	2CLK	-	

NOTES:
- The frequency of CLK (S-7601A clock signal) is twice or more as high as that of SCK.
- Timing is specified at 50% of the signal waveform.
- The rise/fall time (20%, 80%) of the input signal is 15 nsec or less.

Table 5-9 SPI Serial Interface Write/Read Cycle Timing

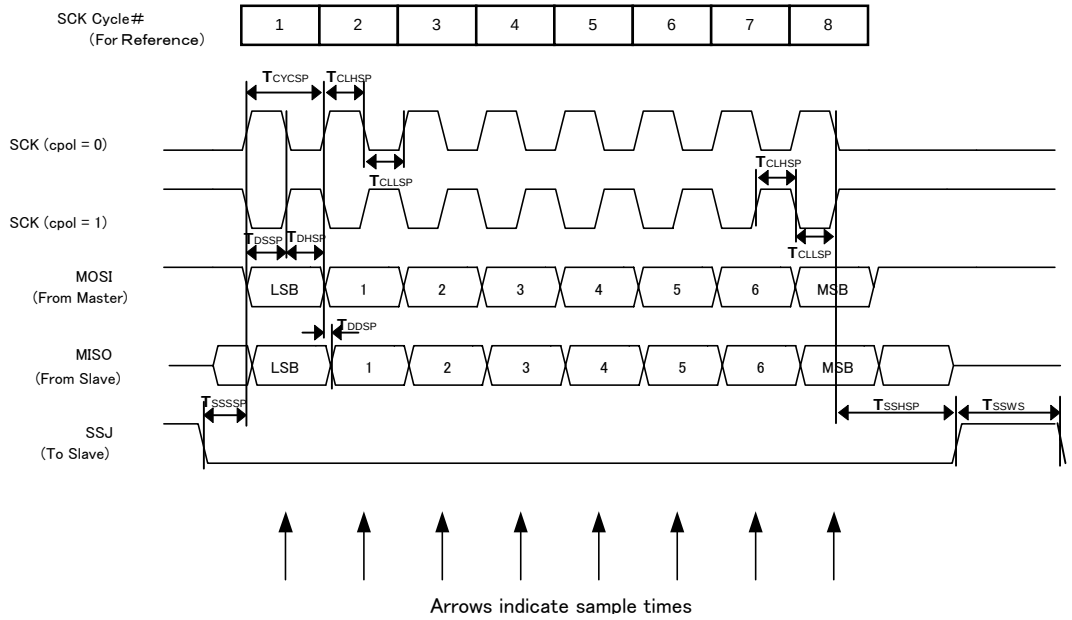


Figure 5-8 SPI Timing (cpha = 1, data order = 1)

Symbol	Description	Min	Max	Notes
T_{CYCSP}	System Cycle Time	250ns	-	
T_{CLLSP}	Clock L Time	40ns	-	
T_{CLHSP}	Clock H Time	40ns	-	
T_{DSSP}	Data Setup Time	20ns	-	
T_{DHSP}	Data Hold Time	20ns	-	
T_{DDSP}	Data Delay Time	-	30ns	CL=80pF
T_{SSSSP}	SSJ Setup Time	2CLK	-	
T_{SSHSP}	SSJ Hold Time	3CLK	-	
T_{SSWSP}	SSJ Disable Time	2CLK	-	

NOTES:
- The frequency of CLK (S-7601A clock signal) is twice or more as high as that of SCK.
- Timing is specified at 50% of the signal waveform.
- The rise/fall time (20%, 80%) of the input signal is 15 nsec or less.

Table 5-10 SPI Serial Interface Write/Read Cycle Timing

5.3.2.3 Transfer Formats

When communicating over the SPI link, the address, data, and cycle type are all multiplexed on the MOSI pin. For read operations, the master first puts an 8 bit address on the bus, followed by the read command (x03) and 2 null bytes. The S-7601A will fetch the data in the third cycle, and return the data in the fourth cycle. These accesses are shown in the following figures.

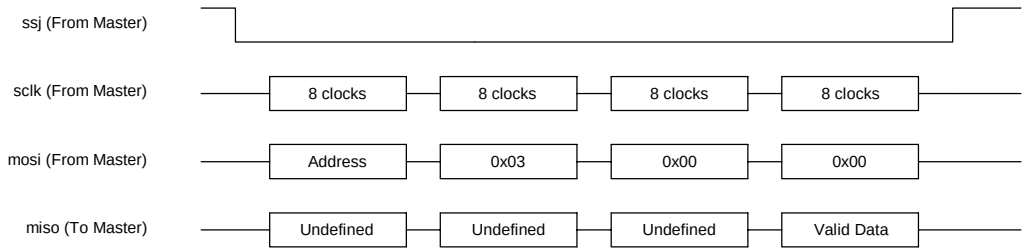


Figure 5-9 SPI Read Cycle

If multiple bytes are to be read from the same register, then the master device can keep issuing read commands till all data is read. The cycle should end with 2 bull bytes regardless of how many data bytes are read. This type of cycle is shown in the following figure.

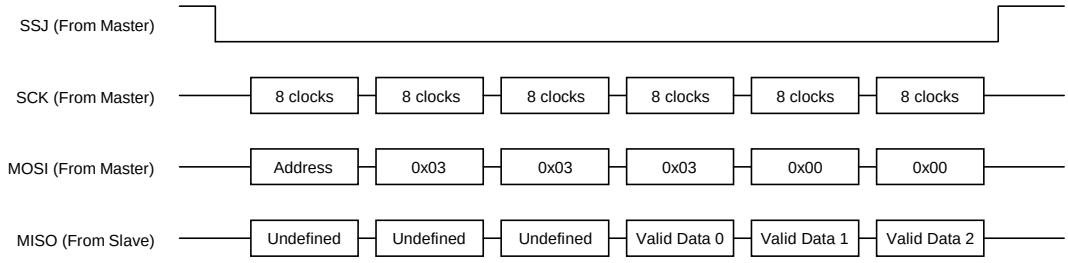


Figure 5-10 SPI Multi Byte Memory Read Cycle

For write cycles, the Master SPI device first puts the desired address on the bus, followed by the write command (0x02), and then the data byte. No data is returned from the chip for write cycles. This format applies to writes to all register locations, and is shown in the following figure.

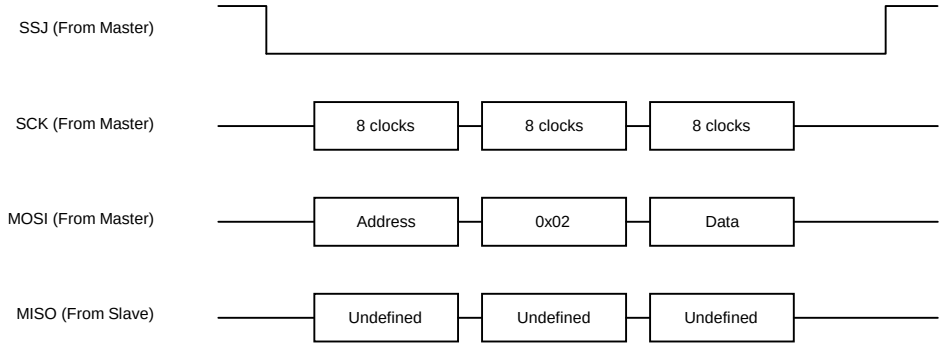


Figure 5-11 SPI Single Byte Write Cycle

For multi-byte write cycles to the same address, the Master can keep writing data after the first write command. This type of cycle is shown in the following figure.

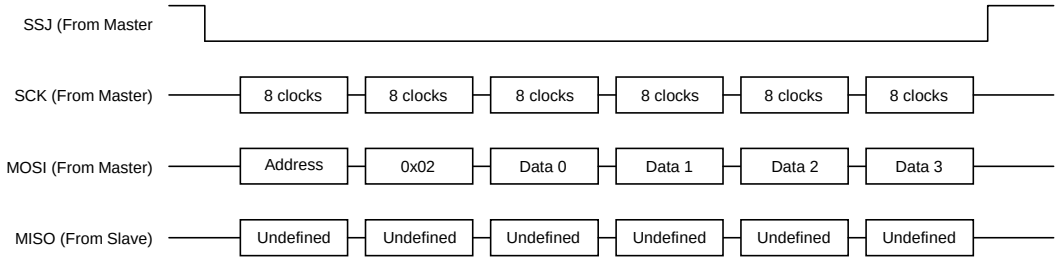


Figure 5-12 SPI Multi Byte Memory Register Write Cycle

5.4 Interrupt

The interrupt signal outputs an active level while the interrupt flag is set in the S-7601A's interrupt register. The interrupt signal returns to an inactive level if the flag clears.
The **INT1** and **INT2X** can be Open Drain or CMOS output depending on the setting of **INTCTL**. The **INT1** and **INT2X** outputs are CMOS if **INTCTL** is "H" otherwise outputs are Open Drain. Table 5-11 defines the interrupt selection.

Interrupt flag	INTCTL	INT1	INT2X
Set	H	H	L
Set	L	H	L
Reset	H	L	H
Reset	L	Hi-Z	Hi-Z

Table 5-11 Interrupt Selection Table

6 Memory Requirements

6.1 Overview

The S-7601A contains two general sockets along with the TCP/UDP/IP and PPP protocols. Their total memory requirement is 12K bytes. This memory is included on the S-7601A chip.

6.2 Memory Interface Architecture

The Network Stack feeds all of its memory requests into a single Memory Arbiter inside of the Network Stack core. The arbiter then feeds out one memory request to the SRAM interface. This interface serves to translate the network stack's timing into signal timing required by the SRAM. This architecture is shown in Figure 6-1.

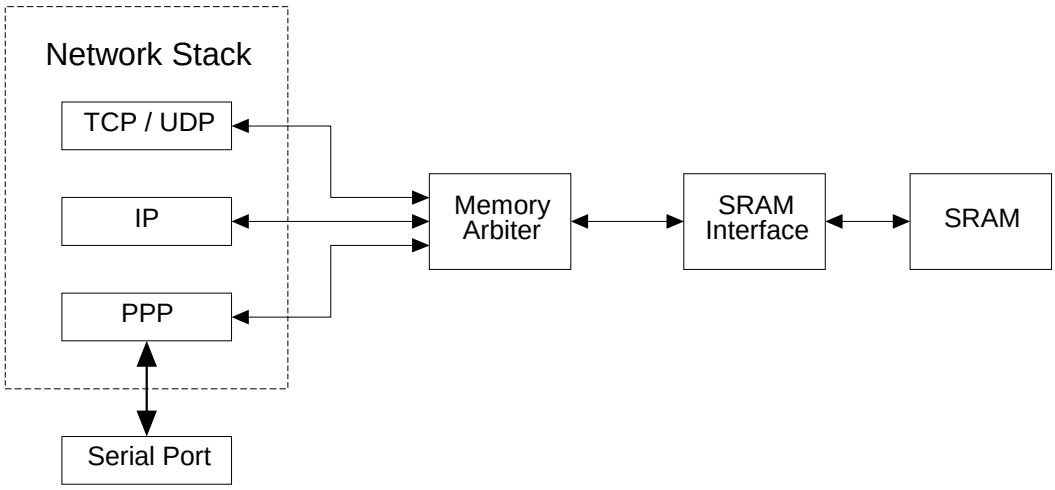


Figure 6-1 Memory Interface Architecture

6.3 Memory Map

The memory map has been configured to make the SRAM supporting the S-7601A compact. The S-7601A has 8K byte and 4K byte memory banks. Their mapping addresses are given in Table 6-1 and Table 6-2.
The actual capacity of the incoming buffer is 2,047 bytes.
The actual capacity of the outgoing buffer is 1,023 bytes.

Table 6-1 S-7601A Memory Map (Bank 0, 8K bytes)

Address	Size	Contents
0x0000 - 0x07FF	2K	Socket 0 Receive Buffer
0x0800 - 0x0FFF	2K	Socket 1 Receive Buffer
0x1000 - 0x13FF	1K	Socket 0 Send Buffer
0x1400 - 0x17FF	1K	Socket 1 Send Buffer
0x1800 - 0x1FFF	2K	IP Buffer

Table 6-2 S-7601A Memory Map (Bank 1, 4K bytes)

Address	Size	Contents
0x000 - 0x7FF	2K	PPP Buffer
0x800 - 0xBFF	1K	PAP/CHAP Buffer
0xC00 - 0xFFF	1K	TCP Data Base

7 S-7601A Register Definitions

7.1 Overview

This section explains the S-7601A's iAPI registers. In the S-7601A , register address mapping is provided by two modes: S-7600A-compatible mode or extended registers mode. The mode is selected via the New_Reg_Mode bit in the general control register. Both iAPI register sets have identical mapping address (0×01). By default, the S-7601A enters S-7600A-compatible mapping mode (New_Reg_Mode=0) after resetting. For both mapping modes, iAPI registers are divided into direct and index registers. Direct registers can be accessed at any time; before index registers can be accessed, the index in the master index register (0×20 for both register mapping modes) must be specified correctly.

7.2 iAPI Register Map

Table 7-1 and Table 7-2 shows the complete iAPI register map for the S-7601A chip. All registers not listed are reserved, and should not be accessed.

Table 7-1 S-7600A-Compatible iAPI Register Map

Add	Register	Bit Definitions							
0x00	Revision	Major Revision Number				Minor Revision Number			
0x01	General_Control	-	-	-	-	-	New Reg	-	SW_ RST
0x02	General_Socket_ Location	-	-	-	-	-	-	S1	S0
0x04	Master_Interrupt	-	-	-	-	-	PT_ INT	LINK _INT	SOCK _INT
0x08	Serial_Port_Config	S_ DAV	DCD	DSR/ HWFC	CTS	RI	DTR	RTS	SCTL
0x09	Serial_Port_Int	PT_ INT	-	-	-	-	-	-	-
0x0A	Serial_Port_Int_ Mask	PINT _EN	DSINT_ EN	DVINT _EN	-	-	-	-	-
0x0B	Serial_Port_Data	Serial Data Register							
0x0C - 0x0D	BAUD_Rate_Div	BAUD Rate Divider Registers							
0x10 - 0x13	Our_IP_Address	Our IP Address							
0x1C	Clock_Div_Low	Low Byte for 1 kHz clock divider							
0x1D	Clock_Div_High	High Byte for 1 kHz clock divider							
0x20	Index	Socket index							
0x21	TOS*	Type of Service Field							
0x22	Socket_ Config_Status_Low*	TO	Buff_ Empty	Buff_ Full	Data_ Avail/ RST	-	Protocol_Type		
0x23	Socket_Status_Mid*	URG	RST	Term	ConU	TCP State			
0x24	Socekt_Activate	-	-	-	-	-	-	S1	S0
0x26	Socket_Interrupt	-	-	-	-	-	-	I1	I0
0x28	Socket_Data_Avail	-	-	-	-	-	-	DAV1	DAV0

NOTE: 1) Reserved bits are signified by a dash (-). All reserved bits should be written as “0”.
2) Indexed registers are signified by an asterisk (*).

Table 7-2 S-7600A-Compatible iAPI Register Map (Continued)

Add	Register	Bit Definitions							
0x2A	Socket_Interrupt_ Mask_Low*	TO_ En	Buff_ Emp_ En	Buff_F ull	Data_ Avail_ En	-	-	-	-
0x2B	Socket_Interrupt_ Mask_High*	URG_En	RST_ En	Term_ En	ConU_ En	-	-	-	-
0x2C	Socket_Interrupt_Low*	TO	Buff_ Empty	Buff_ Full	Data_ Avail	-	-	-	-
0x2D	Socket_Interrupt_High*	URG	RST	Term	ConU	-	-	-	-
0x2E	Socket_Data*	Socket 8-bit data							
0x30	TCP_Data_Send (WO)*	Any write causes data to be sent							
0x30 - 0x31	Buffer_Out (RO)*	Buffer Out Length							
0x32 - 0x33	Buffer_In (RO)*	Buffer In Length							
0x34 - 0x35	Urgent_Data_Pointer*	Urgent Data Offset Pointer							
0x36 - 0x37	Their_Port*	Target Port Address							
0x38 - 0x39	Our_Port*	Our Port Address							
0x3A	Socket_Status_High*	-	-	-	-	-	-	-	Snd _bsy
0x3C - 0x3F	Their_IP_Address*	Target IP Address							
0x60	PPP_Control_Status	PPP_Int	Con_ Val	Use_ PAP	To_ Dis	PPP_ Int_En	Kick	PPP_ En	PPP_ Up / SRset
0x61	PPP_Interrupt_Code	Interrupt Code							
0x62	PPP_Max_Retry	-				PPP Maximum retry			
0x64	PPP_String	Pap user name and password							

NOTE: 1) Reserved bits are signified by a dash (-). All reserved bits should be written as “0”.
2) Indexed registers are signified by an asterisk (*).

7.3 Register Definitions

7.3.1.1 Revision Register (0x00)

(Read-Only, Default 0x22)

This direct read-only register reports back the design revision. See the design revision form in Table 7-3 and Table 7-4.

Table 7-3 Revision Register Bit Definitions

Bit	7	6	5	4	3	2	1	0
Def.	Major Revision Number				Minor Revision Number			
Default	0x2				0x2			

Table 7-4 Revision Register Description

Bit	Bit Name	Access	Description
7:4	Major Revision Number	R	This nibble indicates the major revision number for the network stack core.
3:0	Minor Revision Number	R	This nibble indicates the minor revision number for the network stack core.

NOTE: This number differs from the S-7600A.

7.3.1.2 General Control Register (0x01)

(Read/Write, Default 0x00)

This direct register contains the master software reset. See the register format in Table 7-5 and Table 7-6.

Table 7-5 General Control Register Bit Definitions

Bit	7	6	5	4	3	2	1	0
Def.	-	-	-	-	-	New Reg	-	SW_RST
Default	0	0	0	0	0	0	0	0

NOTE: Reserved bits are signified by a dash (-). All reserved bits should be written as "0."

Table 7-6 General Control Register Description

Bit	Bit Name	Access	Description
2	NewReg	R/W	New Register Mode This bit enables the enhanced new register mapping, and must be set prior to accessing any enhanced new register. By default, this bit comes up 0 after any reset. 0 = S-7600A compatible iAPI Register Map (default) 1 = Enhanced new iAPI Register Map
0	SW_RST	W	Software reset This active high reset returns the S-7601A core to power-on reset settings. It is self-cleaning and does not need to be written to "0" for proper operations. 0 = Normal operation 1 = Soft reset

7.3.1.3 General Socket Location Register (0x02)

(Read-Only)

This register is used to report back the location of general sockets to the software layer. Only bits [1:0] will be set because the S-7601A chip is equipped with two general sockets.

Table 7-7 General Socket Location Register Bit Definitions

Bit	7	6	5	4	3	2	1	0
Def.	-	-	-	-	-	-	S1	S0
Value	0	0	0	0	0	0	1	1

Table 7-8 General Socket Location Register Description

Bit	Bit Name	Access	Description
1	S1	R	General socket 1 available
0	S0	R	General socket 0 available

7.3.1.4 Master Interrupt (0x04)

(Read-Only, Default 0x00)

This direct register indicates the source of the S-7601A interrupt.

Table 7-9 Master Interrupt Register Bit Definitions

Bit	7	6	5	4	3	2	1	0
Def.	-	-	-	-	-	PT_INT	LINK_INT	SOCK_INT
Default	0	0	0	0	0	0	0	0

NOTE: Reserved bits are signified by a dash (-). All Reserved bits should be written as “0”.

Table 7-10 Master Interrupt Register Descriptions (Continued)

Bit	Bit Name	Access	Description
2	PT_INT	R	Physical Transport Interrupt The physical transport triggers this interrupt. An application should check the *Serial Port Int* register to determine the actual cause of the interrupt.
1	LINK_INT	R	Link Layer Interrupt The link layer triggers this interrupt. An application should check the *PPP Interrupt Code* register to determine the actual cause of the interrupt.
0	SOCK_INT	R	Socket Interrupt One of the sockets that need servicing causes this interrupt. An application should check the *Socket Interrupt* register to determine the actual socket number.

7.3.1.5 Serial Port Configuration / Status Register (0x08)

(Read/Write, Default 0X0XX110B)

This register configures the serial port as shown in Table 7-11 and Table 7-12.

Table 7-11 Conf Status Register Bit Definitions

Bit	7	6	5	4	3	2	1	0
Def.	S_DAV	DCD	DSR/ HWFC	CTS	RI	DTR	RTS	SCTL
Default	0	-	0	-	-	1	1	0

Table 7-12 Conf Status Register Description

Bit	Bit Name	Access	Description
7	S_DAV	R/W	Serial Port Data Available When read, this bit indicates that Serial Port data is available. This bit should be written 0.
6	DCD	R/W	Carrier Detect This bit reflects the current state of the **DCD** bit on the serial port. It is independent of the **SCTL** bit setting. This bit should be written 0.
5	DSR / HWFC	R/W	Data Send Ready / Hardware Flow Control When read, this bit reflects the current state of the **DSR** bit on the serial port. When this bit is written: 0 = Hardware Flow control is deactivated 1 = Hardware Flow control activated Refer to Chapter 8 for more information about Hardware Flow Control.
4	CTS	R	Clear To Send This read-only bit reflects the current state of the **CTS** bit on the serial port. It is independent of the **SCTL** bit setting.
3	RI	R	Ring Indicator This read-only bit reflects the current state of the **RI** bit on the serial port. It is independent of the **SCTL** bit setting.
2	DTR	R/W	Data Terminal Ready Reading this bit follows the current state of the **DTR** bit on the serial port. The MPU can control the **DTR** by writing to this bit.
1	RTS	R/W	Request To Send Reading this bit follows the current state of the **RTS** bit on the serial port. The MPU can control the **RTS** by writing to this bit.
0	SCTL	R/W	Serial Port Control This bit determines who controls the serial port. When this bit is low (default), the MPU controls the serial port. When this bit is high, the network stack controls the serial port. 0 = MPU controls serial port 1 = Hardware controls serial port

7.3.1.6 Serial Port Interrupt Register (0x09)

(Read-Only, Default 0X000000B)

This register indicates the state of the serial port interrupt.

Table 7-13 Serial Port Interrupt Register Bit Definitions

Bit	7	6	5	4	3	2	1	0
Def.	PT_INT	-	-	-	-	-	-	-
Default	0	-	0	0	0	0	0	0

NOTE: Reserved bits are signified by a dash (-). All Reserved bits should be written as “0”.

Table 7-14 Serial Port Interrupt Register Description

Bit	Bit Name	Access	Description
7	PT_INT	R	Port Transport Interrupt This bit indicates that the serial port interrupt is active. The operation depends on the status of the PINT_EN, DSINT_EN, and DVINT_EN bits in the Serial Port Interrupt Mask register. PINT_EN is the master enable bit. If PINT_EN is 1, the following combinations enable an interrupt: If DVINT_EN is 1 and data in the serial port receive FIFO is valid, an interrupt always occurs. If DSINT_EN is 1 and the MPU can send one byte of data to the Serial Port Data register, an interrupt occurs. If DVINT_EN and DSINT_EN are both enabled and either condition is met, an interrupt is activated.

NOTE: The control method differs from the S-7600A.

7.3.1.7 Serial Port Interrupt Mask Register (0x0A)

(Read/Write, Default 0x00)

This register enables the serial port interrupts. The default for this register is 0x00 (interrupts disabled).

Table 7-15 Serial Port Interrupt Mask Register Bit Definitions

Bit	7	6	5	4	3	2	1	0
Def.	PINT_EN	DSINT_EN	DVINT_EN	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

NOTE: Reserved bits are signified by a dash (-). All Reserved bits should be written as “0”.

Table 7-16 Serial Port Interrupt Mask Register Description

Bit	Bit Name	Access	Description
7	PINT_EN	R/W	Port Interrupt Enable This is the enable for the port interrupt.
6	DSINT_EN	R/W	Data sent interrupt Enable. This is the enable for the data sent interrupt.
5	DVINT_EN	R/W	Data Available Interrupt Enable. This is the enable for data available interrupt.

7.3.1.8 Serial Port Data Register (0x0B)

(Read/Write)

This register sends data to the serial port (UART) and reads data from the serial port. The data is valid if the S_DAV bit in the Serial Port Config register is set. Data can be written to this register if the PINT_EN and DSINT_EN bits in the Serial Port Interrupt Mask register are set and the PT_INT bit in the Serial Port Interrupt register is set. For more information, see the register description in Table 7-14.

*Note: This register should only be used when the **SCTL** bit in the Serial Port config register is low.*

7.3.1.9 BAUD Rate Divider Registers (0x0C-0x0D)

(Read/Write, Default 0x0000)

These registers set the BAUD rate for the serial port. Calculate the value by using the following formula:

Program Value = [(clk Frequency) / (BAUD Rate)] - 1

Where clk is the clock for the S-7601A core

Example: The clock rate of the S-7601A is 256 KHz and a BAUD rate of 64 Kbps is desired, the programmed value should be:

(256 KHz / 64 k) - 1 = 4 - 1 = 3

Note: The lowest value that should be programmed into these registers is 0x0003.

7.3.1.10 Our IP Address Registers (0x10-0x13)

(Read/Write, Default 0x00000000)

These registers store our IP address or the IP address of the local device. The 0x10 register stores the least significant byte and the 0x13 register stores the most significant byte. If the system controller dose not write an IP address, it will be negotiated for during PPP negotiations (floating IP address). When a PPP connection is established (indicated by bit 0, register 60) these registers can be read to query the IP address obtained.

Table 7-17 Our IP Address Register Bit Definitions (0x10)

Bit	7	6	5	4	3	2	1	0
Def.	Least significant byte of the local IP address							
Default	0x00							

Table 7-18 Our IP Address Register Bit Definitions (0x11)

Bit	7	6	5	4	3	2	1	0
Def.	3rd byte of the local IP address							
Default	0x00							

Table 7-19 Our IP Address Register Bit Definitions (0x12)

Bit	7	6	5	4	3	2	1	0
Def.	2nd byte of the local IP address							
Default	0x00							

Table 7-20 Our IP Address Register Bit Definitions (0x13)

Bit	7	6	5	4	3	2	1	0
Def.	Most significant byte of the local IP address							
Default	0x00							

7.3.1.11 Clock Divider Registers (0x1C-0x1D)

(Read/Write, Default 0x03E7)

These registers program the 1kHz clock generator. This clock is used internally for various S-7601A timing functions. The following equation determines the value programmed into these registers:

(clk Freq/1 kHz) - 1 = Divide Count

Where clk Freq is S-7601A clock frequency. Therefore, for a 1 MHz clock, the divide count equals 1M / 1kHz - 1= 999 = 0x03e7.

7.3.1.12 Index Register (0x20)

(Read/Write, Default 0x00)

This register must be programmed prior to accessing indexed socket registers. Valid programmed values are 0x00 and 0x01. If the selected socket number has not changed since the last access, this register not need to be reprogrammed.

Table 7-21 Index Register Bit Definition

Bit	7	6	5	4	3	2	1	0
Def.	Socket Index [7:0]							
Default	0x00							

Table 7-22 Index Register Description

Bit	Bit Name	Access	Description
7:0	Socket_Index	R/W	0x00 : General Socket 0 Selected 0x01: General Socket 1 Selected All other values are reserved

7.3.1.13 Type of Service Register (TOS) (0x21)

(Read/Write, Default 0x00)

This register configures the TOS field in the IP header for outgoing datagrams. It is an optional setting that defaults to 0x00.

7.3.1.14 Socket Config Status Low Register (0x22)

(Read/Write, Default 0x40)

This register configures the socket.

Table 7-23 Socket Config Status Low Register Bit Definitions

Bit	7	6	5	4	3	2	1	0
Def.	TO	Buff_ Empty	Buff_Full	Data_ Avail / RST	-	Protocol_Type		
Default	0	1	0	0	0	0		

NOTE: Reserved bits are signified by a dash (-). All reserved bits should be written as “0”.

Table 7-24 Socket Config Status Low Register Description

Bit	Bit Name	Access	Description
7	TO	R	TCP Timeout This bit indicates that a TCP timeout condition occurred while attempting to establish a TCP connection or while waiting for a TCP packet after the connection was established. 0 = Normal Operating Condition 1 = Timeout Occurred
6	Buff_Empty	R	This bit indicates whether or not a socket's outgoing data buffer is empty. The bit sets on an empty condition. It then clears and remains clear as long as there is any data in the socket's outgoing data buffer. 0 = Buffer Not Empty 1 = Buffer Empty
5	Buff_Full	R	This bit indicates whether the outgoing buffer is full (1023 bytes or more). It also triggers an interrupt when the outgoing data buffer is full, and the **Buff_Full_En** bit in the *Socket Interrupt Mask Low* register (0x2A) is set. The Data Register should not be written to when this bit is a "1". 0 = Buffer Space Available 1 = No Buffer Space Available
4	Data_Avail / RST	R/W	Writing a "1" to this bit resets all socket parameters to default settings. It is self-clearing and dose not need to be written to low for proper operations. Before resetting, ensure that **Snd_Bsy** bit of *Socket Status High* register (0x3A) is 0. When read, this bit indicates that the socket has data available.
2:0	Protocol_Type	R/W	These bits are used to set the protocol of the socket. All decodes not shown are reserved. 010 = TCP Client Mode 101 = UDP Mode 110 = TCP Server Mode

7.3.1.15 Socket Status Mid Register (0x23)

(Read-Only, Default 0x00)

This read-only register reports other socket status conditions.

Table 7-25 Socket Status Mid Register Bit Definitions

Bit	7	6	5	4	3	2	1	0
Def.	URG	RST	Term	ConU	TCP State			
Default	0	0	0	0	0x0			

Table 7-26 Socket Status Mid Register Description

Bit	Bit Name	Access	Description
7	URG	R	This bit indicates the arrival of urgent data. Writing a "1" to the **URG** bit in the *Socket Interrupt High* register (bit 7) clears this bit. 0 = No urgent data present 1 = Urgent data present
6	RST	R	This bit indicates when the socket receives the RST signal from the TCP peer. 0 = No RST received 1 = RST received
5	Term	R	This bit indicates when the socket terminates from the source and triggers an interrupt if the **Term_En** bit is set in the *Socket Interrupt Mask High* register (0x2B). The interrupt mask setting does not effect the reporting of this status bit. 0 = Normal Operating Condition 1 = Socket terminated from source This bit becomes "1" when the S-7600A receives a TCP segment with the **FIN** flag on. This means that the remote peer has requested to close the TCP connection.
4	ConU	R	This bit indicates when the socket establishes a connection to a host machine. The bit clears when the connection terminates (by either end). 0 = No Connection Established 1 = Connection Established
3:0	TCP State	R	These bits indicate the current TCP state. 0 = CLOSED 1 = SYN_SENT 2 = ESTABLISHED 3 = CLOSE_WAIT 4 = LAST_ACK 5 = FIN_WAIT1 6 = FIN_WAIT2 7 = CLOSING 8 = TIME_WAIT 9 = LISTEN a = SYN_RECVD

7.3.1.16 Socket Activate Register (0x24)

(Read/Write, Default 0x00)

This register is used to activate the sockets and also show the current status of each socket. Setting a bit to “1” activates the corresponding socket. This register defaults to 0x00 upon resets.

Table 7-27 Socket Activate Register Bit Definitions

Bit	7	6	5	4	3	2	1	0
Def.	-	-	-	-	-	-	S1	S0
Default	0	0	0	0	0	0	0	0

Table 7-28 Socket Activate Register Description

Bit	Bit Name	Access	Description
1	S1	R/W	This bit is used to activate general socket 1. 0 = General socket 1 inactive 1 = General socket 1 active
0	S0	R/W	This bit is used to activate general socket 0. 0 = General socket 0 inactive 1 = General socket 0 active

7.3.1.17 Socket Interrupt Register (0x26)

(Read-Only, Default 0x00)

This register indicates which socket has interrupts pending. When identification of an interrupting socket occurs, the actual source of the interrupt is determined by examining the specific socket’s interrupt register.

Table 7-29 Socket Interrupt Register Bit Definitions

Bit	7	6	5	4	3	2	1	0
Def.	-	-	-	-	-	-	I1	I0
Default	0	0	0	0	0	0	0	0

Table 7-30 Socket Interrupt Register Description

Bit	Bit Name	Access	Description
1	I1	R	This bit is used to indicate that socket 1 has an interrupt pending. 0 = General socket 1 interrupt inactive 1 = General socket 1 interrupt active
0	I0	R	This bit is used to indicate that socket 0 has an interrupt pending. 0 = General socket 0 interrupt inactive 1 = General socket 0 interrupt active

7.3.1.18 Socket Data Available Register (0x28)

(Read-Only, Default 0x00)

This read-only register indicates which socket has data pending in the input buffer. A “1” in a bit position indicates that the socket has data available. The bit remains set as long as there is data available.

Table 7-31 Socket Data Avail Register Bit Definitions

Bit	7	6	5	4	3	2	1	0
Def.	-	-	-	-	-	-	DAV1	DAV0
Default	0	0	0	0	0	0	0	0

Table 7-32 Socket Data Avail Register Description

Bit	Bit Name	Access	Description
1	DAV1	R	This bit is used to indicate that socket 1 has data available. 0 = General socket 1 has no data available 1 = General socket 1 has data available
0	DAV0	R	This bit is used to indicate that socket 0 has data available. 0 = General socket 0 has no data available 1 = General socket 0 has data available

7.3.1.19 Socket Interrupt Mask Low Register (0x2A)

(Read/Write, Default 0x00)

This register reports certain interrupt conditions. Setting a bit enables the corresponding interrupt.

Table 7-33 Socket Interrupt Mask Low Register Bit Definitions

Bit	7	6	5	4	3	2	1	0
Def.	TO_En	Buff_ Emp_En	Buff_Full_En	Data_Avail_En	-	-	-	-
Default	0	0	0	0	0	0	0	0

NOTE: Reserved bits are signified by a dash (-). All reserved bits should be written as “0”.

Table 7-34 Socket Interrupt Mask Low Register Description

Bit	Bit Name	Access	Description
7	TO_En	R/W	Writing a “1” enables the Timeout interrupt.
6	Buff_Empty_En	R/W	Writing a “1” enables the Buffer Empty interrupt.
5	Buff_Full_En	R/W	Writing a “1” enables the Buffer Full interrupt.
4	Data_Avail_En	R/W	Writing a “1” enables the Data Available interrupt.

7.3.1.20 Socket Interrupt Mask High Register (0x2B)

(Read/Write, Default 0x00)

This register enables certain types of interrupt conditions. Setting bits enables their corresponding interrupts.

Table 7-35 Socket Interrupt Mask High Register Bit Definitions

Bit	7	6	5	4	3	2	1	0
Def.	URG_En	RST_En	Term_En	ConU_En	-	-	-	-
Default	0	0	0	0	0	0	0	0

NOTE: Reserved bits are signified by a dash (-). All reserved bits should be written as “0”.

Table 7-36 Socket Interrupt Mask High Register Description

Bit	Bit Name	Access	Description
7	URG_En	R/W	Writing a “1” to enable the Urgent Data interrupt.
6	RST_En	R/W	Writing a “1” to enable the Connection Reset interrupt.
5	Term_En	R/W	Writing a “1” to enable the Socket Termination interrupt.
4	ConU_En	R/W	Writing a “1” to enable the Connection Up interrupt.

7.3.1.21 Socket Interrupt Low Register (0x2C)

(Read/Write, Default 0x00)

This register reports certain interrupt conditions. When an interrupt condition occurs and its enable bit is set, the hardware sets the corresponding bit. Writing a "1" to the bit clears it. Disabling the corresponding enable bit prevents the interrupt from showing.

Table 7-37 Socket Interrupt Low Register Bit Definitions

Bit	7	6	5	4	3	2	1	0
Def.	TO	Buff_Emplty	Buff_Full	Data_Avail	-	-	-	-
Default	0	0	0	0	0	0	0	0

NOTE: Reserved bits are signified by a dash (-). All reserved bits should be written as “0”.

Table 7-38 Socket Interrupt Low Register Description

Bit	Bit Name	Access	Description
7	TO	R/W	This interrupt is generated when a timeout condition occurred while trying to establish a connection. Writing a “1” to this bit clears the interrupt.
6	Buff_Empty	R/W	This interrupt is generated when outgoing buffer is empty. Writing a “1” to this bit clears the interrupt.
5	Buff_Full	R/W	This interrupt is generated when the outgoing buffer is full (1023 bytes). Writing a “1” to this bit clears the interrupt.
4	Data_Avail	R/W	This interrupt is generated when data is available from the incoming buffer. Writing a “1” to this bit clears the interrupt.

7.3.1.22 Socket Interrupt High Register (0x2D)

(Read/Write, Default 0x00)

This register reports certain interrupt conditions. When an interrupt condition occurs and its enable bit is set, the hardware sets the corresponding bit. Writing a "1" to the bit clears it. Disabling the corresponding enable bit prevents the interrupt from showing.

Table 7-39 Socket Interrupt High Register Bit Definitions

Bit	7	6	5	4	3	2	1	0
Def.	URG	RST	Term	ConU	-	-	-	-
Default	0	0	0	0	0	0	0	0

NOTE: Reserved bits are signified by a dash (-). All reserved bits should be written as “0”.

Table 7-40 Socket Interrupt High Register Description

Bit	Bit Name	Access	Description
7	URG	R/W	This interrupt is generated when urgent data arrives. The system interface should read the *Urgent Data Pointer* register to see the location of the data. Writing a “1” to this bit clears the interrupt.
6	RST	R/W	This interrupt is generated when a TCP peer sends the socket RST flag indicating that the current TCP session is not valid. Writing a “1” to this bit clears this interrupt. When this condition occurs, the hardware no longer operates and re-initializing the socket is recommended.
5	Term	R/W	This interrupt is generated when the socket connection is terminated and a TCP FIN flag is received. Writing a “1” to this bit clears the interrupt.
4	ConU	R/W	This interrupt is generated when a connection is established. Writing a “1” to this bit clears the interrupt.

7.3.1.23 Socket Data Register (0x2E)

(Memory Mapped Read/Write, Default 0x00)

This register is used by a system controller to read incoming data packets and write outgoing data. Data transmissions start for TCP connections only after a write occurs at 0x30.

7.3.1.24 TCP Data Send and Buffer Out Length Registers (0x30-0x31)

(Read/Write, Default 0x03FF)

When read, these registers report the amount of space available in the outgoing buffer. Register 0x30 stores the least significant byte; 0x31 stores the most significant byte. Writing any data to 0x30 causes data transmissions to start on TCP connections.

7.3.1.25 Buffer In Length Registers (0x32-0x33)

(Read-Only, Default 0x0000)

These read-only registers report the amount of data available in the received data buffer. 0x32 stores the least significant byte; 0x33 stores the most significant byte.

7.3.1.26 Urgent Data Pointer Registers (0x34-0x35)

(Read-Only, Default 0x0000)

These read-only registers report the offset to the start of urgent data (as marked through the TCP header) relative to the incoming data buffer. Register 0x34 stores the least significant byte; 0x35 stores the most significant byte.

7.3.1.27 Their Port Registers (0x36-0x37)

(Read/Write, Default 0x0000)

These registers specify the destination port for an outgoing data packets. For TCP client or UDP mode, this value must be set prior to activating the socket. For TCP server mode, the port number transmitted from Peer at the time of connection is put into these registers automatically. Register 0x36 stores the least significant byte and 0x37 stores the most significant byte.

Table 7-41 Their Port Register Bit Definitions (0x36)

Bit	7	6	5	4	3	2	1	0
Def.	Least significant byte of the target port number							
Default	0x00							

Table 7-42 Their Port Register Bit Definitions (0x37)

Bit	7	6	5	4	3	2	1	0
Def.	Most significant byte of the target port number							
Default	0x00							

7.3.1.28 Our Port Registers (0x38-0x39)

(Read/Write, Default 0x0000)

These registers are used it indicate the source port for an outgoing data packet. When setting a TCP client or sending data using UDP, these registers should be set to the proper value. Normally in client applications, the software increments the value of this register. The TCP/UDP server application should set these registers to be the value used by the server applications. Register 0x38 stores the least significant byte; 0x39 stores the most significant byte.

Table 7-43 Our Port Register Bit Definitions (0x38)

Bit	7	6	5	4	3	2	1	0
Def.	Least significant byte of the local port number							
Default	0x00							

Table 7-44 Our Port Register Bit Definitions (0x39)

Bit	7	6	5	4	3	2	1	0
Def.	Most significant byte of the local port number							
Default	0x00							

7.3.1.29 Socket Status High Register (0x3A)

(Read-Only, Default 0x00)

This register reports the busy status of the socket.

Table 7-45 Socket Status High Register Bit Definitions

Bit	7	6	5	4	3	2	1	0
Def.	-	-	-	-	-	-	-	Snd_Bsy
Default	0	0	0	0	0	0	0	0

NOTE: Reserved bits are signified by a dash (-). All reserved bits should be written as “0”.

Table 7-46 Socket Status High Register Description

Bit	Bit Name	Access	Description
0	Snd_Bsy	R	This bit indicates that the current socket is busy sending TCP segments. Before the socket is reset, this bit should be 0. 0 = Socket not busy 1 = Socket busy

7.3.1.30 Their IP Address Registers (0x3C-0x3F)

(Read/Write, Default 0x00000000)

These registers indicate the destination IP address for the socket. For TCP client or UDP mode, this value must be set prior to activating the socket. For TCP server mode, the IP address transmitted from Peer at the time of connection is put into these registers automatically.The registers can be written in any order.

Table 7-47 Their IP Address Register Bit Definitions (0x3C)

Bit	7	6	5	4	3	2	1	0
Def.	Least significant byte of Destination IP address							
Default	0x00							

Table 7-48 Their IP Address Register Bit Definitions (0x3D)

Bit	7	6	5	4	3	2	1	0
Def.	3rd byte of Destination IP address							
Default	0x00							

Table 7-49 Their IP Address Register Bit Definitions (0x3E)

Bit	7	6	5	4	3	2	1	0
Def.	2nd byte of Destination IP address							
Default	0x00							

Table 7-50 Their IP Address Register Bit Definitions (0x3F)

Bit	7	6	5	4	3	2	1	0
Def.	Most significant byte of Destination IP address							
Default	0x00							

7.3.1.31 PPP Control and Status Register (0x60)

(Read/Write, Default 0x00)

This register control the PPP layer and reports its status.

Table 7-51 PPP Control and Status Register Bit Definitions (0x60)

Bit	7	6	5	4	3	2	1	0
Def.	PPP_Int	Con_Val	Use_ PAP	TO_Dis	PPP_Int_En	Kick	PPP_En	PPP_Up /SRst
Default	0	0	0	0	0	0	0	0

Table 7-52 PPP Control Status Register Description

Bit	Bit Name	Access	Description
7	PPP_Int	R/W	PPP Interrupt This bit indicates that the PPP triggered an interrupt condition. Read the PPP interrupt code register to determine the cause. Writing a “1” to this bit position clears the interrupt.
6	Con_Val	R/W	Connection Valid This bit indicates to the network stack that the underlying connection is up and valid. 0 = Connection down (default) 1 = Connection up
5	Use_PAP	R/W	This bit enables PAP authentication within the PPP protocol. If enabled, a PAP request is issued after PAP authentication is negotiated. The PAP string enters through register 0x64. 0 = PAP disabled (default) 1 = PAP enabled
4	TO_Dis	R/W	A "0" must be written to this bit for using as testing.
3	PPP_Int_En	R/W	PPP Interrupt Enable This bit enables the PPP interrupt. 0 = PPP Interrupt disabled (default) 1 = PPP Interrupt enabled
2	Kick	W	A "0" must be written to this bit for using as testing.
1	PPP_En	R/W	PPP Enable This bit enables the PPP layer. The bit must be set before any transmissions occur. 0 = PPP disabled (default) 1 = PPP enabled

Bit	Bit Name	Access	Description
0	PPP_UP/SRst	R/W	When read, this bit indicates when the PPP layer establishes a connection. 0 = PPP Connection down 1 = PPP Connection established When written, this bit will reset the PPP engine. It is self-clearing and goes not need to be written low for normal operations. 0 = PPP Normal operation 1 = PPP Reset

7.3.1.32 PPP Interrupt Code (0x61)

(Read-Only, Default 0x00)

This register indicates the interrupt condition that causes the PPP interrupt to trigger.

Table 7-53 PPP Interrupt Code Register Bit Definitions

Bit	7	6	5	4	3	2	1	0
Def.	PPP Interrupt Code							
Default	0							

Table 7-54 PPP Interrupt status Codes

Status Code	Definition
0x00	Reserved
0x01	PPP Failed initial LCP negotiations
0x02	PPP Failed NCP negotiations
0x05	PAP Failed negotiations
0x09	PPP up
0x0A	PPP down

NOTE: Other status codes are reserved. The status codes 0x09 and 0x0A are added to the S-7600A. The status codes 0x09 and 0x0A are also the interruption factors of PPP.

7.3.1.33 PPP Max Retry, (0x62)

(Read/Write, Default 0x0A)

This register configures the maximum retry number. This number is used to determine the maximum number of configuration requests that are sent during the PPP negotiation stage.

Table 7-55 PPP Max Retry Register

Bit	7	6	5	4	3	2	1	0
Def.	-				PPP Maximum Retry			
Default	0x0				0xA			

NOTE: Reserved bits are signified by a dash (-).

7.3.1.34 PAP String (0x64)

(Write-Only)

This write-only register enters the string for the PAP configuration request packet. Enter the string according to the format shown Table 7-56.

Table 7-56 PAP String Format

Byte	String
[0]	Length of username
[1]	First byte of username
[2]	Second byte of username
[n]	Last byte of username (where n is the length of the username string)
[n+1]	Length of password
[n+2]	First byte of password
[n+m+1]	Last byte of password (where m is the length of the password string)

As an example, if the username string is “joe” and the password is “public”, enter the bytes as shown inTable 7-57.

Table 7-57 PAP String Example

byte:0	0x03	Length of username string
byte:1	0x6a	Character “j”
byte:2	0x6f	Character “o”
byte:3	0x65	Character “e”
byte:4	0x06	Length of password string
byte:5	0x70	Character “p”
byte:6	0x75	Character “u”
byte:7	0x62	Character “b”
byte:8	0x6C	Character “l”
byte:9	0x69	Character “i”
byte:a	0x63	Character “c”

If PAP is used, the **Use_PAP** bit must be set in the *PPP Control and Status* register (0x60) prior to entering the PAP string.

7.4 Enhanced new iAPI Register Map

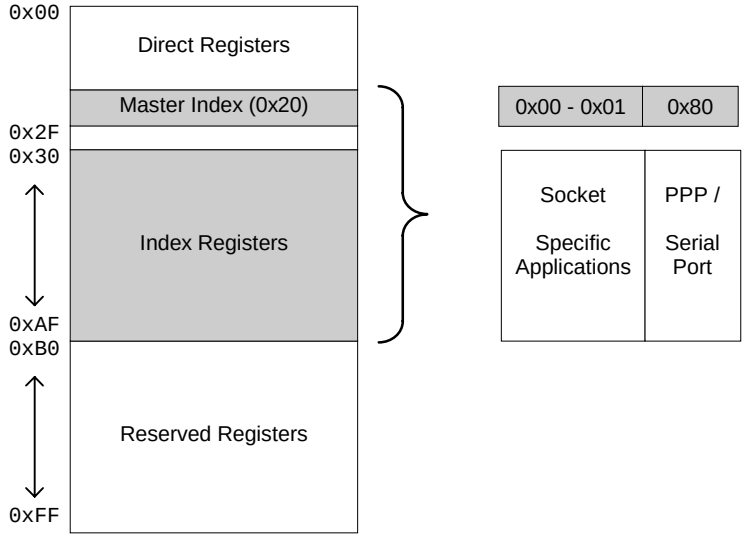
7.4.1 Enhanced new iAPI Register Map Overview

Enhanced new iAPI registers are divided into two types: direct and indexed.

Direct registers occupy the address space from 0x00 to 0x2F. The direct registers can be accessed without initializing the Master Index register.

Indexed registers occupy the register space from 0x30 to 0xAF. Indexed registers require the Master Index Register (0x20) to be set with the appropriate value before accessing the desired bank of registers. See Figure 7-1.

Figure 7-1 Top Level Register Map



7.4.2 Enhanced new iAPI Register Map

Table 7-58 shows the complete iAPI Register Map for Enhanced S-7601A. Unlisted registers are reserved and should not be accessed.

Table 7-58 iAPI Register Map

Add	Register	Bit Definitions							
0x00	Revision	Major Revision Number (0x02)				0Minor Revision Number (0x02)			
0x01	General_Control	-	-	-	-	-	New_Reg	-	SW_Rst
0x02	General_Socket_Location	-	-	-	-	-	-	S1	S0
0x04	Master_Interrupt	-	-	-	-	-	PT_Int	Link_Int	Sock_Int
0x1C	Clock_Div_Low	Low byte for 1 kHz clock divider							
0x1D	Clock_Div_High	High byte for 1 kHz clock divider							
0x20	Master Index	Index value of the registers to be accessed							
0x24	Socket_Activate	Activates sockets						S1	S0
0x26	Socket_Interrupt	Socket interrupt statuses						I1	I0
0x28	Socket_Data_Avail	Socket data available						DAV1	DAV0
0x30-0xAF	Indexed	Indexed registers							
0xB0-0xFF	Reserved	Reserved registers							

NOTES: Reserved bits are signified by a dash (-). All reserved bits should be written as “0”.

The General Sockets uses the following registers. Prior to accessing these registers, the Master index register should be programmed with either 0x00 (for socket 0) or 0x01 (for socket 1).

Table 7-59 Index Registers used by General Sockets

iAPI	Register Name	Register Definition							
0x30	App_ID	Application ID (0x10)							
0x31	Revision	Revision (0x27)							
0x32	Configuration	-	-	-	-	-	Type		
0x34	Status 0	TO	Snd_Emp	-	Rcv_Dav	-	-	-	-
0x35	Status 1	Urg	Rcv_Rst	Rcv_Fin	Con_Up	-	-	-	-
0x36	Interrupt Enable 0	TO_En	Snd_EmpEn	-	Rcv_DavEn	-	-	-	-
0x37	Interrupt Enable 1	Urg_En	Rcv_RstEn	Rcv_FinEn	Con_UP_En	-	-	-	-
0x38	Interrupt Status 0	TO	Snd_Emp	-	Rcv_Dav	-	-	-	-
0x39	Interrupt Status 1	Urg	Rcv_Rst	Rcv_Fin	Con_Up	-	-	-	-
0x3A	Socket Command	-	-	-	Sck_Clr	-	-	-	Send_Go
0x3C	Socket Data	Socket Data							
0x44 – 0x47	Remote IP Address	Remote IP Address							
0x48 – 0x49	Local Port	Local Port							
0x4A – 0x4B	Remote Port	Remote Port							
0x4C – 0x4D	Buffer Length Out	Buffer Length Out							
0x4E – 0x4F	Buffer Length In	Buffer Length In							
0x51	Delayed ACK Control	Delayed ACK Timer							
0x53	TOS	TOS							
0x54 – 0x55	Urgent Pointer	Urgent Pointer							
0x56 – 0x57	MSS	Maximum Segment Size							
0x5A	Status 2	-	-	-	Sck_Busy	TCP State			
0x5C – 0x5D	TCP Clk Divider	TCP Clock Divider							
0x5E	TCP Clk Enable	-	-	-	-	-	-	-	CLKEn

The PPP module uses the following registers. Prior to accessing these registers, the Master index register should be programmed with 0x80.

Table 7-60 PPP Register Map

iAPI	Register Name	Register Definition							
0x30	App_ID	Application ID (0x01)							
0x31	Revision	Revision (0x15)							
0x32	PPP_Ctrl_Stat	PPP_Int	Con_Val	Use_PAP	TO_Dis	PPP_Int_En	Kick	PPP_En	PPP_Up/Rst
0x38	PPP_Int_Code	PPP interrupt code							
0x3C	PPP_Data	PPP data							
0x3D	PAP_String	PAP username and password							
0x3E	PPP_Max_Retry	IPAD	Use_CHAP	PPP_Buf	PAP_Rst	Max_Retry			
0x3F	CHAP_Ctrl_Stat	CHAP_Dav	CHAP_Nak	CHAP_Ack	-	Chal_Int_En	Nak_Int_En	Ack_Int_En	-
0x40-0x43	Local_IP_Addr	Local IP address							
0x44-0x45	PPP_Prot	PPP protocol for transmitted packets							
0x46	CHAP_ID	Code ID from CHAP packets							
0x48-0x4B	Peer_IP_Add	Peer IP address							
0x4E-0x4F	PPP_Data_Len	Length of the PPP data available to be read							
0x50	PPP_State	NCP state				LCP state			
0x52-0x53	MRU	MRU of peer							
0x71	SP_Rev	Serial Port revision(0x20)							
0x72	SP_Config	-	-	HWFC	CTS	-	DTR	RTS	SCTL
0x73	SP_Status	Data_Av	DCD	DSR	CTS	RI	DTR	RTS	SCTL
0x76	SP_Int_Enable	PInt_En	DSInt_En	DVInt_En	DCD IntEn	-	-	-	-
0x78	SP_Int	PInt	DSInt	DVInt	DCD Int	-	-	-	-
0x7C	SP_Data	Serial port data							
0x80-0x81	SP_BAUD_Rate_Div	BAUD Rate for the Serial Port							

NOTE: Reserved bits are signified by a dash (-). All reserved bits should be written as “0”.

7.5 Enhanced new iAPI Register Definitions

7.5.1 Direct Registers

The direct registers can be accessed without initializing the Master Index register.

7.5.1.1 Revision Register—0x00

(Read-only, Default 0x22)

This register reports back the design revision. See the design revision form in the following tables.

Table 7-61 Revision Register Bit Definitions

Bit	7	6	5	4	3	2	1	0
Definition	Major Revision Number				Minor Revision Number			
Default	0x2				0x2			

Table 7-62 Revision Register Description

Bit	Bit Name	Access	Description
7:4	Major Revision Number	R	This nibble indicates the major revision number for the Network Stack core.
3:0	Minor Revision Number	R	This nibble indicates the minor revision number for the Network Stack core.

7.5.1.2 General Control Register—0x01

(Read / Write, Default 0x00)

This register contains the master software reset. See the register format in the following tables.

Table 7-63 General Control Register Bit Definitions

Bit	7	6	5	4	3	2	1	0
Definition	-	-	-	-	-	NewReg	-	SW_Rst
Default	0	0	0	0	0	0	0	0

NOTE: Reserved bits are signified by a dash (-). All reserved bits should be written as “0”.

Table 7-64 General Control Register Description

Bit	Bit Name	Access	Description
2	NewReg	R/W	New Register Mode This bit enables the enhanced new register mapping, and must be set prior to accessing any enhanced new register. By default, this bit comes up 0 after any reset. 0 = S-7600A compatible iAPI Register Map (default) 1 = Enhanced new iAPI Register Map
0	SW_Rst	W	Software Reset This active high reset returns the Network Stack core to power-on reset settings. It is self-clearing and does not need to be written to “0” for proper operations. 0 = Normal operation 1 = Soft reset

7.5.1.3 General Socket Location Register—0x02

(Read-only, Default 0x03)

These registers report back the location of general sockets to the software layer. Any bit position containing a "1" indicates that a general socket is available at that particular slot.

Table 7-65 General Socket Location Low Register Bit Definitions (0x02)

Bit	7	6	5	4	3	2	1	0
Definition	-	-	-	-	-	-	S1	S0
Default	0	0	0	0	0	0	1	1

Table 7-66 Generic Socket Location Register Description

Bit	Bit Name	Access	Description
1	S1	R	GenSock 1 available
0	S0	R	GenSock 0 available

7.5.1.4 Master Interrupt Register—0x04

(Read-only, Default 0x00)

This register indicates the source of the S-7601A interrupt.

Table 7-67 Master Interrupt Register Bit Definitions

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Definition	-	-	-	-	-	PT_Int	Link_Int	Sock_Int
Default	0	0	0	0	0	0	0	0

NOTE: Reserved bits are signified by a dash (-). All reserved bits should be written as “0”.

Table 7-68 Master Interrupt Register Description

Bit	Bit Name	Access	Description
2	PT_Int	R	Physical Transport Interrupt The physical transport triggers this interrupt. An application should check the Serial Port Interrupt Register (0x78) to determine the actual cause of the interrupt.
1	Link_Int	R	Link Layer Interrupt The link layer triggers this interrupt. An application should check the PPP Interrupt Code Register (0x38) to determine the actual cause of the interrupt.
0	Sock_Int	R	Socket Interrupt A socket that needs servicing causes this interrupt. An application should check the Socket Interrupt Register (0x26) to determine the actual socket number.

7.5.1.5 Clock Divider Registers—0x1C-0x1D

(Read/Write, Default 0x03E7)

These registers program a 1kHz clock generator. This clock is used internally for various Network Stack timing functions. The following equation determines the value programmed into these registers:

(clk Freq/1kHz) – 1 = Divide Count

Where clk Freq, is the clock frequency of the S-7601A. Therefore, for a 1 MHz input clock, the divide count equals 1M / 1kHz - 1= 999 = 0x03e7.

Table 7-69 Clock Divider Register [Clock_Div_Low] Bit Definitions (0x1C)

Bit	7	6	5	4	3	2	1	0
Definition	Least Significant Byte (LSB) of Divide Count							
Default	0xE7							

Table 7-70 Clock Divider Register [Clock_Div_High] Bit Definitions (0x1D)

Bit	7	6	5	4	3	2	1	0
Definition	Most Significant Byte (MSB) of Divide Count							
Default	0x03							

7.5.1.6 Master Index Register—0x20

(Read/Write, Default 0x00)

This register must be programmed prior to accessing indexed registers. If the index number has not changed since the last access, the register does not need to be reprogrammed.

Table 7-71 Master Index Register Bit Definitions

Bit	7	6	5	4	3	2	1	0
Definition	MSB of Divide Count							
Default	0x00							

Table 7-72 Master Index Register Description

Bit	Bit Name	Access	Description
7:0	Master Index	R/W	Index of the registers to be accessed.

Table 7-73 Valid Index Values

Index	Registers Accessed
0x00 – 0x01	Socket 0 – Socket 1
0x80	PPP and Serial Port

7.5.1.7 Socket Activate Register—0x24

(Read/Write, Default 0x00)

This register activates a socket and provides its active/inactive status. Setting a bit to “1” activates the corresponding socket. This register defaults to 0x00 upon reset. The format for this register is shown in the following table.

Table 7-74 Socket Activate Low Register Bit Definitions (0x24)

Bit	7	6	5	4	3	2	1	0
Definition	-	-	-	-	-	-	S1	S0
Default	0	0	0	0	0	0	0	0

NOTE: Reserved bits are signified by a dash (-). All reserved bits should be written as "0".

7.5.1.8 Socket Interrupt Register—0x26

(Read-only, Default 0x00)

This direct register indicates which sockets have interrupts pending. The actual source of the interrupt can be determined by examining the Interrupt Status Register (see Indexed Registers) of the appropriate socket.

Table 7-75 Socket Interrupt Register Bit Definitions (0x26)

Bit	7	6	5	4	3	2	1	0
Definition	-	-	-	-	-	-	I1	I0
Default	0	0	0	0	0	0	0	0

NOTE: Reserved bits are signified by a dash (-). All reserved bits should be written as "0".

7.5.1.9 Socket Data Available Registers—0x28

(Read-only, Default 0x00)

This register indicates which sockets have data pending in the receive buffer. A “1” in a bit position indicates that the socket has data available to be read. The bit will remain set as long as there is data available to be read.

Table 7-76 Socket Data Available Low Register Bit Definitions (0x28)

Bit	7	6	5	4	3	2	1	0
Definition	-	-	-	-	-	-	DAV1	DAV0
Default	0	0	0	0	0	0	0	0

NOTE: Reserved bits are signified by a dash (-). All reserved bits should be written as "0".

7.5.2 Indexed Registers

Indexed registers can be accessed by first programming the Master Index Register (0x20) with the required value for the desired register bank.

7.5.3 Socket Register Overview

The socket registers allow the host CPU to communicate with the Network Stack core when using UDP or TCP. The socket operation uses direct registers such as Socket Activate and Socket Interrupt registers. The socket indexed registers listed in Table 7-77 should only be accessed after setting the proper value (in this case, the value would be 0x00 or 0x01) to the Master Index Register (0x20). The following table summarizes the indexed registers used by general sockets.

Table 7-77 Index Registers used by General Sockets

iAPI	Register Name	Register Definition							
0x30	App_ID	Application ID (0x10)							
0x31	Revision	Revision (0x27)							
0x32	Configuration	-	-	-	-	-	Type		
0x34	Status 0	TO	Snd_ Emp	-	Rcv_ Dav	-	-	-	-
0x35	Status 1	Urg	Rcv_ Rst	Rcv_ Fin	Con_ Up	-	-	-	-
0x36	Interrupt Enable 0	TO_E n	Snd_ EmpE n	-	Rcv_ DavE n	-	-	-	-
0x37	Interrupt Enable 1	Urg_E n	Rcv_ RstEn	Rcv_ FinEn	Con_ UP_E n	-	-	-	-
0x38	Interrupt Status 0	TO	Snd_ Emp	-	Rcv_ Dav	-	-	-	-
0x39	Interrupt Status 1	Urg	Rcv_ Rst	Rcv_ Fin	Con_ Up	-	-	-	-
0x3A	Socket Command	-	-	-	Sck_ Clr	-	-	-	Send_ Go
0x3C	Socket Data	Socket Data							
0x44 – 0x47	Remote IP Address	Remote IP Address Registers							
0x48 – 0x49	Local Port	Local Port							
0x4A – 0x4B	Remote Port	Remote Port							
0x4C – 0x4D	Buffer Length Out	Buffer Length Out							
0x4E – 0x4F	Buffer Length In	Buffer Length In							
0x51	Delayed ACK Time	Delayed ACK Timer							
0x53	TOS	TOS							
0x54 – 0x55	Urgent Pointer	Urgent Pointer							
0x56 – 0x57	MSS	Maximum Segment Size							

iAPI	Register Name	Register Definition							
0x5A	Status 2	-	-	-	Sck_ Busy	TCP State			
0x5C – 0x5D	TPC Clk Divider	TCP Clock Divider							
0x5E	TCP CLK En	-	-	-	-	-	-	-	Clk_En

7.5.4 Socket Register Definitions

7.5.4.1 Socket Application ID Register—0x30

(Read-only, Default 0x10)

This register reports back the application ID value. The general socket ID is 0x10.

Table 7-78 Socket Application ID Register Bit Definitions

Bit	7	6	5	4	3	2	1	0
Definition	Socket Application ID							
Default	0	0	0	1	0	0	0	0

7.5.4.2 Socket Revision Register—0x31

(Read-only, Default 0X27)

This register reports back the revision of the general socket. The general socket revision is 0x27.

Table 7-79 Socket Revision Register Bit Definitions

Bit	7	6	5	4	3	2	1	0
Definition	Socket Revision							
Default	0	0	1	0	0	1	1	1

7.5.4.3 Socket Configuration Register—0x32

(Read/Write, Default 0x00)

This register configures the socket type, and indicates particular status conditions of the socket. This register is defined as shown in the following tables.

Table 7-80 Socket Configuration Register Bit Definitions

Bit	7	6	5	4	3	2	1	0
Definition		-	-	-	-	Type		
Default	0	0	0	0	0	0		

NOTE: Reserved bits are signified by a dash (-). All reserved bits should be written as “0”.

Table 7-81 Socket Configuration Register Description

Bit	Bit Name	Access	Description
2:0	Type	R/W	These bits define the protocol of the socket as follows: 000 = Reserved (default) 001 = UDP Client Mode 010 = TCP Client Mode 011 = Reserved 100 = Reserved 101 = UDP Raw Mode 110 = TCP Server Mode 111 = Reserved In UDP Raw mode, the application is presented with the remote IP address and the UDP header information along with the UDP data. In UDP Client Mode, only the data portion is presented to the application. In all TCP modes, only the data portion of the TCP packet is presented to the application.

7.5.4.4 Socket Status 0 Register—0x34

(Read-only, Default 0x40)

This register indicates status conditions of the socket, and is defined in the following tables. All of the bits in this register are unaffected by the state of the Interrupt Enable register bits.

Table 7-82 Socket Status 0 Register Bit Definitions

Bit	7	6	5	4	3	2	1	0
Definition	TO	Snd_Emp	-	Rcv_Dav	-	-	-	-
Default	0	1	0	0	0	0	0	0

NOTE: Reserved bits are signified by a dash (-). All reserved bits should be written as “0”.

Table 7-83 Socket Status 0 Register Description

Bit	Bit Name	Access	Description
7	TO	R	Timeout This bit indicates that the socket has timed out and triggers an interrupt if the TO_En bit is set in the Interrupt Enable 0 Register (0x36). This bit is cleared when the software writes to the Sck_Clr bit in the Command Register (0x3A). 0 = Normal operating condition 1 = Connection timed out
6	Snd_Emp	R	Send Buffer Empty This bit indicates whether or not a socket’s Send Buffer is empty. It sets upon an empty condition, and clears and remains clear if there is any data in the socket’s Send Buffer. 0 = Buffer not empty 1 = Buffer empty
4	Rcv_Dav	R	Receive Data Available This bit indicates that the socket has data available to be read in the Receive Buffer. This bit is cleared when all of the data has been read. 0 = No data available 1 = Data available

7.5.4.5 Socket Status 1 Register—0x35

(Read-only, Default 0x00)

This register indicates additional status conditions of the socket, and is defined as shown in the following tables. All of the bits in this register are unaffected by the state of the Interrupt Enable register bits.

Table 7-84 Socket Status 1 Register Bit Definitions

Bit	7	6	5	4	3	2	1	0
Definition	Urg	Rcv_Rst	Rcv_Fin	Con_Up	-	-	-	-
Default	0	0	0	0	0	0	0	0

NOTE: Reserved bits are signified by a dash (-). All reserved bits should be written as “0”.

Table 7-85 Socket Status 1 Register Description

Bit	Bit Name	Access	Description
7	Urg	R	Urgent Data Present This bit indicates when urgent data has been received. It is cleared automatically when the Urgent Pointer Registers (0x54-0x55) become "0". 0 = No urgent data present 1 = Urgent data present
6	Rcv_Rst	R	Receive Reset Segment This bit indicates that the socket has received a reset flag during a TCP session. Upon reception of this flag the hardware will not receive any more data from its peer. Therefore, the software needs to reinitialize this socket because the current session is considered disabled. This bit is cleared when the software writes a “0” to the Sck_Clr bit in the Command Register (0x3A). 0 = Normal operating condition 1 = Socket reset by peer
5	Rcv_Fin	R	Receive Fin This bit indicates when the peer terminates the TCP connection. This bit is cleared when the software writes a “0” to the Sck_Clr bit in the Command Register (0x3A). 0 = Normal operating condition 1 = Socket terminated from peer
4	Con_Up	R	Connection Up This bit indicates that the socket has established a connection to a host machine. The bit clears when either end terminates the connection. 0 = No connection established 1 = Connection established

7.5.4.6 Socket Interrupt Enable 0 Register—0x36

(Read/Write, Default 0x00)

This register enables different types of interrupt conditions. When a bit is set the corresponding interrupt is enabled. This register must be written prior to activating the sockets. This register defaults to 0x00 upon reset, and is defined in the following tables.

Table 7-86 Socket Interrupt Enable 0 Register Bit Definitions

Bit	7	6	5	4	3	2	1	0
Definition	TO_En	Snd_Emp_En	-	Rcv_Dav_En	-	-	-	-
Default	0	0	0	0	0	0	0	0

NOTE: Reserved bits are signified by a dash (-). All reserved bits should be written as “0”.

Table 7-87 Socket Interrupt Enable 0 Register Description

Bit	Bit Name	Access	Description
7	TO_En	R/W	Timeout Interrupt Enable 0 = Interrupt disabled (Default) 1 = Interrupt enabled
6	Snd_Emp_En	R/W	Send Buffer Empty Interrupt Enable 0 = Interrupt disabled (Default) 1 = Interrupt enabled
4	Rcv_Dav_En	R/W	Receive Data Available Interrupt Enable 0 = Interrupt disabled (Default) 1 = Interrupt enabled

7.5.4.7 Socket Interrupt Enable 1 Register—0x37

(Read/Write, Default 0x00)

This register enables specific types of interrupt conditions. When a bit is set, the corresponding interrupt is enabled. This register must be written prior to activating the sockets. This register defaults to 0x00 upon reset, and is defined in the following tables.

Table 7-88 Socket Interrupt Enable 1 Register Bit Definitions

Bit	7	6	5	4	3	2	1	0
Definition	Urg_En	Rcv_Rst_E	Rcv_Fin_En	Con_Up_E	-	-	-	-
Default	0	0	0	0	0	0	0	0

NOTE: Reserved bits are signified by a dash (-). All reserved bits should be written as “0”.

Table 7-89 Socket Interrupt Enable 1 Register Description

Bit	Bit Name	Access	Description
7	Urg_En	R/W	Urgent Data Present Interrupt Enable 0 = Interrupt disabled (Default) 1 = Interrupt enabled
6	Rcv_Rst_En	R/W	Receive Reset Segment Interrupt Enable 0 = Interrupt disabled (Default) 1 = Interrupt enabled
5	Rcv_Fin_En	R/W	Receive Fin Interrupt Enable 0 = Interrupt disabled (Default) 1 = Interrupt enabled
4	Con_Up_En	R/W	Connection Up Interrupt Enable 0 = Interrupt disabled (Default) 1 = Interrupt enabled

7.5.4.8 Socket Interrupt Status 0 Register—0x38

(Read/Write, Default 0x00)

This register indicates specific interrupt conditions. A bit is set to "1" when the corresponding event occurs and is enabled by the Interrupt Enable Register 0 (0x36). This register defaults to 0x00 upon reset, and is defined in the following tables.

Table 7-90 Socket Interrupt Status 0 Register Bit Definitions

Bit	7	6	5	4	3	2	1	0
Definition	TO	Snd_Emp	-	Rcv_Dav	-	-	-	-
Default	0	0	0	0	0	0	0	0

NOTE: Reserved bits are signified by a dash (-). All reserved bits should be written as “0”.

Table 7-91 Socket Interrupt Status 0 Register Description

Bit	Bit Name	Access	Description
7	TO	R/W	Timeout Interrupt Status This interrupt indicates that a timeout condition occurred while trying to establish a connection. This status is cleared by writing a “1” to this bit.
6	Snd_Emp	R/W	Send Buffer Empty Interrupt Status This interrupt indicates that the Send Buffer is empty. This status is cleared by writing a “1” to this bit.
4	Rcv_Dav	R/W	Receive Data Available Interrupt Status This interrupt indicates that data is available to be read in the Receive Buffer. This status is cleared by writing a "1" to this bit.

7.5.4.9 Socket Interrupt Status 1 Register—0x39

(Read/Write, Default 0x00)

This register indicates specific interrupt conditions. A bit is set to "1" when the corresponding interrupt occurs and is enabled by the Interrupt Enable Register 1 (0x37). This register defaults to 0x00 upon reset, and is defined in the following tables.

Table 7-92 Socket Interrupt Status 1 Register Bit Definitions

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Definition	Urg	Rcv_Rst	Rcv_Fin	Con_Up	-	-	-	-
Default	0	0	0	0	0	0	0	0

NOTE: Reserved bits are signified by a dash (-). All reserved bits should be written as “0”.

Table 7-93 Socket Interrupt Status 1 Register Description

Bit	**Bit Name**	**Access**	**Description**
7	Urg	R/W	Urgent Data Present Interrupt Status This interrupt indicates that an Urgent flag has arrived. This bit is cleared by writing a "1" to it.
6	Rcv_Rst	R/W	Receive Reset Segment Interrupt Status This interrupt indicates that the socket has received a Reset flag during a TCP session. When this condition occurs, the S-7601A no longer operates and re-initializing the socket is recommended. This bit is cleared by writing a "1" to it.
5	Rcv_Fin	R/W	Receive Fin Interrupt Status This interrupt indicates that the socket has received a Fin flag during a TCP session. This bit is cleared by writing a "1" to it.
4	Con_Up	R/W	Connection Up Interrupt Status This interrupt indicates that a connection has been established. This bit is cleared by writing a "1" to it.

7.5.4.10 Socket Command Register—0x3A

(Write-only, Default 0x00)

This register is used by software to clear a socket and to initiate a data send.

Table 7-94 Socket Command Register Bit Definitions

Bit	7	6	5	4	3	2	1	0
Definition	-	-	-	Sck_Clr	-	-	-	Send_Go
Default	0	0	0	0	0	0	0	0

NOTE: Reserved bits are signified by a dash (-). All reserved bits should be written as “0”.

Table 7-95 Socket Command Register Description

Bit	Bit Name	Access	Description
4	Sck_Clr	W	Socket Clear Writing a "1" to this bit clears the socket. It is recommended that software clear the socket before using it. Before issuing this command, the software should ensure that the Sck_Busy bit in the Socket Status 2 Register (bit 4,0x5A) is not "1". This command should also be used after receiving a RST segment from a TCP peer. This bit is self-clearing.
0	Send_Go	W	Send Go Writing a "1" to this bit causes the socket to send data after writing the transmit data through the data register. This bit is self-clearing. In TCP mode, the hardware automatically segments data stored in the Send Buffer. In UDP mode, this bit causes stored data to be sent out. The software should not send data larger than the size of the link layer MRU. See section 8.2(TCP/UDP Data Communications).

7.5.4.11 Socket Data Register—0x3C

(Read/Write, Default N/A)

This register reads data from the Receive Buffer and writes data into the Send Buffer.

Table 7-96 Socket Data Register Bit Definitions

Bit	7	6	5	4	3	2	1	0
Definition	Socket Data							
Default	N/A							

Table 7-97 Socket Data Register Description

Bit	Bit Name	Access	Description
7:0	Socket Data	R/W	Writing a byte to this register causes the socket to store it in the socket's Send Buffer. The socket sends data when the software issues a *Send_Go* command through the Command Register (0x3A). Reading this register causes the socket to provide received data until the *Rcv_Dav* bit in Status Register 0 (0x34) becomes "0".

7.5.4.12 Remote IP Address Registers—0x44–0x47

(Read/Write, Default 0x00000000)

These registers are used to indicate the destination IP address for the socket and must be setup prior to activating the socket except for TCP server and UDP receive modes. During TCP server mode, the peer sets these registers after the connection is established. These registers may be written in any order and are defined as shown in the following tables.

Table 7-98 Remote IP Address 0 Register Bit Definitions (0x44)

Bit	7	6	5	4	3	2	1	0
Definition	LSB of Destination IP Address							
Default	0x00							

Table 7-99 Remote IP Address 1 Register Bit Definitions (0x45)

Bit	7	6	5	4	3	2	1	0
Definition	Third Byte of Destination IP Address							
Default	0x00							

Table 7-100 Remote IP Address 2 Register Bit Definitions (0x46)

Bit	7	6	5	4	3	2	1	0
Definition	Second Byte of Destination IP Address							
Default	0x00							

Table 7-101 Remote IP Address 3 Register Bit Definitions (0x47)

Bit	7	6	5	4	3	2	1	0
Definition	MSB of Destination IP Address							
Default	0x00							

7.5.4.13 Local Port Registers—0x48–0x49

(Read/Write, Default 0x0000)

These registers indicate the source port for an outgoing packet. When sending data using the TCP client or UDP mode, these registers should be set to a value not used by well-known services. Normally in client applications, the software should increment the value of this register for each session. The TCP and UDP server applications should set these registers to be the value used by the server.

Table 7-102 Local Port Low Register Bit Definitions (0x48)

Bit	7	6	5	4	3	2	1	0
Definition	LSB of Local Port							
Default	0x00							

Table 7-103 Local Port High Register Bit Definitions (0x49)

Bit	7	6	5	4	3	2	1	0
Definition	MSB of Local Port							
Default	0x00							

7.5.4.14 Remote Port Registers—0x4A–0x4B

(Read/Write, Default 0x0000)

These registers indicate the destination port for an outgoing packet. This value is used in the TCP header, and must be set up prior to activating the socket. These registers do not need to be set when using the socket for TCP server or UDP receive software applications. When using the socket as a TCP server, these registers are automatically set after the connection is established and will contain the port number of the remote client.

Table 7-104 Remote Port Low Register Bit Definitions (0x4A)

Bit	7	6	5	4	3	2	1	0
Definition	LSB of Remote Port							
Default	0x00							

Table 7-105 Remote Port High Register Bit Definitions (0x4B)

Bit	7	6	5	4	3	2	1	0
Definition	MSB of Remote Port							
Default	0x00							

7.5.4.15 Buffer Length Out Registers—0x4C–0x4D

(Read-only, Default 0x03FF)

These registers are used to report the amount of space available in the Send Buffer. If the Send Buffer is empty, the value of these registers is 0x03FF. The software should always first read the Buffer Length Out High Register, and then read the Buffer Length Out Low Register. These registers default to 0x03FF upon reset. See section 8.2(TCP/UDP Data Communications).

Table 7-106 Buffer Length Out Low Register Bit Definitions (0x4C)

Bit	7	6	5	4	3	2	1	0
Definition	Buffer Length Out[7:0]							
Default	0xFF							

Table 7-107 Buffer Length Out High Register Bit Definitions (0x4D)

Bit	7	6	5	4	3	2	1	0
Definition	-	-	-	-	-	-	Buffer Length Out[9:8]	
Default	0x03							

7.5.4.16 Buffer Length In Registers—0x4E–0x4F

(Read-only, Default 0x0000)

These registers report the amount of data available to be read from the Receive Buffer. If the Receive Buffer is empty, the value of these registers is 0x0000.The software should always first read the Buffer Length In High Register, and then read the Buffer Length In Low Register. These registers default to 0x0000 upon reset. See section 8.2(TCP/UDP Data Communications).

Table 7-108 Buffer Length In Low Register Bit Definitions (0x4E)

Bit	7	6	5	4	3	2	1	0
Definition	Buffer Length In [7:0]							
Default	0x00							

Table 7-109 Buffer Length In High Register Bit Definitions (0x4F)

Bit	7	6	5	4	3	2	1	0
Definition	-	-	-	-	-	Buffer Length In [10:8]		
Default	0x00							

7.5.4.17 Delayed Ack Control Register—0x51

(Read/Write, Default 0x00)

This register sets the time interval used in delayed acks as defined in the following tables.

Table 7-110 Delayed Ack Control Bit Definitions (0x51)

Bit	7	6	5	4	3	2	1	0
Definition	Delayed Ack Time							
Default	0x00							

Table 7-111 Delayed Ack Control Register Description (0x51)

Bit	Bit Name	Access	Description
7:0	Delayed Ack Time	R/W	This field sets the delay time in milliseconds (ms). The delay time can be programmed from 0 to 255 ms. The default value is 0 ms.

7.5.4.18 Type of Service Register—0x53

(Read/Write, Default 0x00)

This register configures the TOS field in the IP header for sending datagrams. This bit location correspond to TOS field.

Table 7-112 TOS Register Bit Definitions

Bit	7	6	5	4	3	2	1	0
Definition	Type Of Service							
Default	0X00							

7.5.4.19 Urgent Pointer Registers—0x54–0x55

(Read/Write, Default 0x00)

These registers report the offset to the start of urgent data (as marked via the TCP header) relative to the Receive Buffer. When a TCP socket receives an *Urgent flag*, it triggers an interrupt if enabled and the socket status will indicate that the flag was received. When socket data is read through the data register, the value indicated by these registers decrements with each read. If a new urgent pointer is received before the urgent data is read, all of these registers are overwritten with new data. The Network Stack is incapable of sending urgent data.

Table 7-113 Urgent Pointer Low Register Bit Definitions (0x54)

Bit	7	6	5	4	3	2	1	0
Definition	LSB of Urgent Pointer							
Default	0x00							

Table 7-114 Urgent Pointer High Register Bit Definitions (0x55)

Bit	7	6	5	4	3	2	1	0
Definition	MSB of Urgent Pointer							
Default	0x00							

7.5.4.20 Maximum Segment Size (MSS) Registers—0x56–0x57

(Read/Write, Default 0x0218)

These registers are used to report the TCP MSS value requested by a TCP peer. The default value of MSS after initializing the socket is 536. If the TCP peer requests a different MSS value, these registers are updated. Software can also overwrite these values, but it is not recommended to use values greater than those read.

Table 7-115 MSS Low Register Bit Definitions (0x56)

Bit	7	6	5	4	3	2	1	0
Definition	LSB of MSS							
Default	0x18							

Table 7-116 MSS High Register Bit Definitions (0x57)

Bit	7	6	5	4	3	2	1	0
Definition	MSB of MSS							
Default	0x02							

7.5.4.21 Socket Status 2 Register—0x5A

(Read-only, Default 0x00)

This register indicates status conditions of the socket, and is defined as shown in the following tables. The bits in this register are unaffected by the state of the Interrupt Enable register bits.

Table 7-117 Socket Status 2 Register Bit Definitions

Bit	7	6	5	4	3	2	1	0
Definition	-	-	-	Sck_Busy	TCP State			
Default	0	0	0	0	0x0			

NOTE: Reserved bits are signified by a dash (-). All reserved bits should be written as “0”.

Table 7-118 Socket Status 2 Register Description

Bit	Bit Name	Access	Description
4	Sck_Busy	R	Socket Busy This bit indicates that the current socket is busy sending or receiving TCP segments. The socket is reset by writing a “1” to Socket Command Register (bit4, 0x3A). The software should ensure that this bit is 0 before re-setting the socket. 0 = Socket not busy 1 = Socket busy
3:0	TCP State	R	These bits indicate the current TCP state. 0 = Closed 1 = Syn_Sent 2 = Established 3 = Close_Wait 4 = Last_ACK 5 = Fin_Wait1 6 = Fin_Wait2 7 = Closing 8 = Time_Wait 9 = Listen a = Syn_Recvd

7.5.4.22 TCP Clock Divider Registers—0x5C - 0x5D

(Read/Write, Default 0x03E7)

These registers program an optional TCP clock generator. This clock is used internally for various TCP timing functions. In order to use this clock, the TCP clock enable bit in register 0x5E must be enabled. Otherwise the global 1 kHz clock is used for the TCP module. The follow equation determines the value programmed into these registers:

(clk Freq / tcp_clk) – 1 = Divide Count

Where clk Freq, is the clock frequency of the chip, and tcp_clk is the desired rate for the TCP module. Therefore, for a 1 MHz input clock and a desired TCP clock rate of 1kHz, the divide count equals 1M / 1kHz – 1 = 999 = 0x03e7. For normal network conditions, the TCP divider should be set to produce a 1 kHz clock for tcp_clk.

Table 7-119 TCP Clock Divider Register but Definitions (0x5C)

Bit	7	6	5	4	3	2	1	0
Definition	Least Significant Byte (LSB) of Divide Count							
Default	0xE7							

Table 7-120 TCP Clock Divider Register but Definitions (0x5D)

Bit	7	6	5	4	3	2	1	0
Definition	Most Significant Byte (MSB) of Divide Count							
Default	0x03							

7.5.4.23 TCP Clock Enable Register—0x5E

(Read/Write, Default 0x00)

This register is used to enable the separate timer clock used for the TCP module. If this feature us not enabled, then the TCP module will use the 1 kHz clock as derived from the Clock Divider registers (0x1C, 0x1D). If it is enabled, then it uses he clock as derived form the TCP Clock Divider registers (0x5C, 0x5D). This register is only available when the socket index is set to 0x00, but will affect all sockets.

Table 7-121 TCP Clock Enable Register Bit Definitions

Bit	7	6	5	4	3	2	1	0
Definition	Reserved							Clk_En
Default	0x00							0x0

Table 7-122 TCP Clock Enable Register Description

Bit	Bit Name	Access	Description
0	Clk_En	R/W	TCP Clock enable 0 = TCP uses 1 kHz clock (default) 1 = TCP uses separate TCP timer clock

7.5.5 PPP / Serial Port Registers

7.5.5.1 PPP / Serial Port Register Map

The Master Index Register must be programmed to 0x80 prior to accessing the PPP and Serial Port indexed registers. All registers above 0x30 are indexed.

Table 7-123 PPP Register Map

iAPI	Register Name	Register Definition							
0x30	App_ID	Application ID (0x01)							
0x31	Revision	Revision (0x15)							
0x32	PPP_Ctrl_Stat	PPP_Int	Con_Val	Use_PAP	TO_Dis	PPP_Int_En	Kick	PPP_En	PPP_Up/Rst
0x38	PPP_Int_Code	PPP interrupt code							
0x3C	PPP_Data	PPP data							
0x3D	PAP_String	PAP username and password							
0x3E	PPP_Max_Retry	IPAD	Use_CHAP	PPP_Buf	PAP_Rst	Max_Retry			
0x3F	CHAP_Ctrl_Stat	CHAP_Dav	CHAP_Nak	CHAP_Ack	-	Chal_Int_En	Nak_Int_En	Ack_Int_En	-
0x40-0x43	Local_IP_Addr	Local IP address							
0x44-0x45	PPP_Prot	PPP protocol for transmitted packets							
0x46	CHAP_ID	Code ID from CHAP packets							
0x48-0x4B	Peer_IP_Add	Peer IP address							
0x4E-0x4F	PPP_Data_Len	Length of the PPP data available to be read							
0x50	PPP_State	NCP state				LCP state			
0x52-0x53	MRU	MRU of peer							
0x71	SP_Rev	Serial Port revision(0x20)							
0x72	SP_Config	-	-	HWFC	CTS	-	DTR	RTS	SCTL
0x73	SP_Status	Data_Av	DCD	DSR	CTS	RI	DTR	RTS	SCTL
0x76	SP_Int_Enable	PInt_En	DSInt_En	DVInt_En	DCD IntEn	-	-	-	-
0x78	SP_Int	PInt	DSInt	DVInt	DCD Int	-	-	-	-
0x7C	SP_Data	Serial port data							
0x80-0x81	SP_BAUD_Rate_Div	BAUD Rate for the Serial Port							

NOTE: Reserved bits are signified by a dash (-). All reserved bits should be written as “0”.

7.5.6 PPP / Serial Port Register Definitions

7.5.6.1 PPP Application ID Register—0x30

(Read-only, Default 0x01)

This register reports back the application ID for the PPP engine. This value is fixed at 0x01.

Table 7-124 Application ID Register Bit Definitions

Bit	7	6	5	4	3	2	1	0
Definition	PPP Application ID							
Default	0	0	0	0	0	0	0	1

7.5.6.2 PPP Revision ID Register—0x31

(Read-only, Default 0x15)

This register reports back the revision ID for the PPP engine. This value is currently at 0x15.

Table 7-125 Revision ID Register Bit Definitions

Bit	7	6	5	4	3	2	1	0
Definition	PPP Revision							
Default	0	0	0	1	0	1	0	1

7.5.6.3 PPP Control and Status Register—0x32

(Read/Write, Default 0x00)

This register controls the PPP layer and reports its status.

Table 7-126 PPP Control and Status Register Bit Definitions

Bit	7	6	5	4	3	2	1	0
Definition	PPP_Int	Con_Val	Use_PAP	TO_Dis	PPP_Int_En	Kick	PPP_En	PPP_Up/SRst
Default	0	0	0	0	0	0	0	0

Table 7-127 PPP Control and Status Register Description

Bit	Bit Name	Access	Description
7	PPP_Int	R/W	PPP Interrupt This bit indicates that PPP triggered an interrupt condition. Read the PPP Interrupt Code Register (0x38) to determine the cause. Writing a “1” to this bit clears the interrupt. 0 = PPP interrupt inactive 1 = PPP interrupt active
6	Con_Val	R/W	Connection Valid This bit indicates to the Network Stack that the underlying physical connection is up and valid. When written a “1” to PPP_En bit in this register, this bit should be written a “1” as same time. Ensure that the PPP connection is terminated before writing a “0” to this bit. 0 = Connection down (default) 1 = Connection up
5	Use_PAP	R/W	Use PAP Authentication This bit enables PAP authentication within the PPP protocol. If enabled, a PAP request is issued if PAP authentication is negotiated. The PAP string is entered through the PAP String Register (0x3D). This bit must be set prior to entering the PAP string. If CHAP is enabled also, the PPP engine may request and use CHAP regardless of this bit's setting. 0 = PAP disabled (default) 1 = PAP enabled
4	TO_Dis	R/W	A “0” must be written to this bit for using as testing.
3	PPP_Int_En	R/W	PPP Interrupt Enable This bit enables the PPP interrupt. 0 = PPP Interrupt disabled (default) 1 = PPP Interrupt enabled
2	Kick	R/W	A “0” must be written to this bit for using as testing.
1	PPP_En	R/W	PPP Enable This bit enables the PPP layer. The bit must be set before any PPP transmissions occur. When written a “1” to Con_Val bit in this register, this bit should be written a “1” as same time. 0 = PPP disabled (default) 1 = PPP enabled

Bit	Bit Name	Access	Description
0	PPP_Up/SRst	R/W	PPP Up / Soft Reset When read, this bit indicates when the PPP layer establishes a connection. 0 = PPP connection down 1 = PPP connection established When written, this bit will reset the PPP engine. It is self-clearing and does not need to be written low for normal operations. Ensure that the PPP connection is terminated before writing a “1” to this bit. 0 = PPP normal operation 1 = PPP reset

7.5.6.4 PPP Interrupt Code Register—0x38

(Read-only, Default 0x00)

This register indicates the interrupt condition that caused the PPP interrupt to trigger. The PPP interrupt status codes are shown below.

Table 7-128 PPP Interrupt Code Register Bit Definitions

Bit	7	6	5	4	3	2	1	0
Definition	PPP Interrupt Status Code							
Default	0x00							

Table 7-129 PPP Interrupt Status Codes

Status Code	Definition
0x00	Reserved
0x01	PPP failed LCP negotiations
0x02	PPP failed NCP negotiations
0x04	Termination request received
0x05	PAP failed negotiations
0x06	CHAP challenge received
0x07	CHAP Ack received
0x08	CHAP Nak received
0x09	PPP up
0x0A	PPP down

7.5.6.5 PPP Data Register—0x3C

(Read/Write, Default N/A)

This register reads CHAP challenge data and writes CHAP response packets. Prior to reading this register, the CPU should query the PPP Data Length Registers (0x4E-0x4F) to determine how much data is available to be read.

Prior to writing this register, the software application should ensure that the PPP_Buf bit in the PPP Max Retry Register (bit 5, 0x3E) is set. After writing a CHAP packet to this register, the CPU should write 0x00 to the LSB of the PPP Data Length Register (0x4E). This write will trigger transmission of the packet.

Table 7-130 PPP Data Register Bit Definitions

Bit	7	6	5	4	3	2	1	0
Definition	PPP Data							
Default	N/A							

7.5.6.6 PAP String Register—0x3D

(Read/Write, Default N/A)

This register enters the string for the PAP configuration request packet. The string is entered by multiple consecutive writes to this register. Enter the string according to the format shown in the following table.

Table 7-131 PAP String Format

Byte	String
[0]	Length of username
[1]	First byte of username
[2]	Second byte of username
[n]	Last byte of username (where “n” is the length of the username string)
[n+1]	Length of password
[n+2]	First byte of password
[n+m+1]	Last byte of password (where “m” is the length of the password string)

As an example, if the username string is “joe” and the password is “public”, enter the bytes as shown in the following table.

Table 7-132 PAP String Example

Byte	Value	Comment
0	0x03	Length of username string
1	0x6a	Character “j”
2	0x6f	Character “o”
3	0x65	Character “e”
4	0x06	Length of password string
5	0x70	Character “p”
6	0x75	Character “u”
7	0x62	Character “b”
8	0x6c	Character “l”
9	0x69	Character “i”
a	0x63	Character “c”

If PAP is used, the Use_PAP bit must be set in the PPP Control and Status Register (0x32) prior to entering the PAP string.

7.5.6.7 PPP Max Retry Register—0x3E

(Read/Write, Default 0x2A)

This register controls various PPP parameters and reports various status bits.

Table 7-133 PPP Max Retry Register Bit Definitions

Bit	7	6	5	4	3	2	1	0
Definition	IPAD	Use_CHAP	PPP_Buf	PAP_Rst	Max_Retry			
Default	0	0	1	0	0x0A			

Table 7-134 PPP Max Retry Register Description

Bit	Bit Name	Access	Description
7	IPAD	R/W	IP Address Assignment Mode Enable This bit enables the IP Address Assignment mode. 0 = Client Mode (default) 1 = IP Address Assignment Mode
6	Use_CHAP	R/W	Use CHAP This bit enables CHAP authentication within the PPP negotiations. If enabled and the host requests the CHAP protocol, CHAP challenge packets will be presented to the software as they arrive. *Note: Setting this bit does NOT guarantee use of the CHAP protocol. It is also legal and probably desirable to set the Use_PAP bit as well.* 0 = CHAP disabled (default) 1 = CHAP enabled
5	PPP_Buf	R/W	PPP Buffer Clear This read-only bit indicates that the data written to the PPP_Data register has been sent out. 0 = PPP Data being sent 1 = PPP Data buffer empty
4	PAP_Rst	W	PAP String Reset This write-only bit is used to reset the PAP string register. Prior to writing that register, this bit should be set. It is self-clearing, and need not be written low for normal operations. 0 = Normal operation 1 = Reset PAP register
3:0	Max_Retry	R/W	Max Retry This field is used to indicate to the PPP layer how many configuration requests it should attempt before determining that the negotiations have failed. By default this field is set to 0xA (11 retries because a 0 based counter is used.) This setting is consistent with RFC recommendations.

7.5.6.8 CHAP Control and Status Register—0x3F

(Read/Write, Default 0x00)

This register controls various CHAP parameters and reports various status bits.

Table 7-135 CHAP Control and Status Register Bit Definitions

Bit	7	6	5	4	3	2	1	0
Definition	CHAP_Dav	CHAP_Nak	CHAP_Ack	-	Chal_Int_En	Nak_Int_En	Ack_Int_En	-
Default	0	0	0	0	0	0	0	0

NOTE: Reserved bits are signified by a dash (-). All reserved bits should be written as “0”.

Table 7-136 CHAP Control and Status Register Description

Bit	Bit Name	Access	Description
7	CHAP_Dav	R/W	CHAP Data Available This bit indicates that a CHAP challenge packet has been received and the data is available for the CPU to read. If the *Chal_Int_En* bit is set, this condition will trigger a PPP interrupt. Writing "1" to this bit clears the status and interrupt. This interrupt can also be cleared by writing a "1" to the *PPP_Int* bit in the PPP Control and Status Register (0x32). 0 = No data available (default) 1 = CHAP challenge data available
6	CHAP_Nak	R/W	CHAP Nak Received This bit indicates that a CHAP Nak packet was received. If the *Nak_Int_En* bit is also set, this condition triggers a PPP interrupt. Writing this bit to a "1" clears the status and the interrupt. The interrupt can also be cleared by writing a “1” to the *PPP_Int* bit in the PPP Control and Status Register (0x32). 0 = Normal condition (default) 1 = CHAP Nak received
5	CHAP_Ack	R/W	CHAP Ack Received This bit indicates that a CHAP Ack packet was received. If the *Ack_Int_En* bit is also set, this condition triggers a PPP interrupt. Writing this bit to a "1" clears the status and interrupt. The interrupt can also be cleared by writing a “1” to the *PPP_Int* bit in the PPP Control and Status Register (0x32). 0 = Normal condition (default) 1 = CHAP Ack received
3	Chal_Int_En	R/W	Challenge Interrupt Enable This bit enables an interrupt when a CHAP challenge packet is received. The state of this bit has no effect on the value to read back from the *CHAP_Dav* bit in this register. 0 = Challenge interrupt disabled (default) 1 = Challenge interrupt enabled

Bit	Bit Name	Access	Description
2	Nak_Int_En	R/W	Nak Interrupt Enable This bit enables an interrupt when a CHAP Nak packet is received. The state of this bit has no effect on the value to read back from the *CHAP_Nak* bit in this register. 0 = Nak interrupt disabled (default) 1 = Nak interrupt enabled
1	Ack_Int_En	R/W	Ack Interrupt Enable This bit enables an interrupt when a CHAP ACK packet is received. The state of this bit has no effect on the value to read back from the *CHAP_Ack* bit in this register. 0 = ACK interrupt disabled (default) 1 = ACK interrupt enabled

7.5.6.9 Local IP Address Registers—0x40-0x43

(Read/Write, Default 0x00000000)

These registers store the IP address of the local device. If an IP address is not entered, it will be obtained during PPP negotiations (floating IP address). When a PPP connection is established (indicated by bit 0, register 0x32) these registers can be read to query the obtained IP address.

Table 7-137 Local IP Address Register Bit Definitions (0x40)

Bit	7	6	5	4	3	2	1	0
Definition	LSB of the local IP address							
Default	0x00							

Table 7-138 Local IP Address Register Bit Definitions (0x41)

Bit	7	6	5	4	3	2	1	0
Definition	Third byte of the local IP address							
Default	0x00							

Table 7-139 Local IP Address Register Bit Definitions (0x42)

Bit	7	6	5	4	3	2	1	0
Definition	Second byte of the local IP address							
Default	0x00							

Table 7-140 Local IP Address Register Bit Definitions (0x43)

Bit	7	6	5	4	3	2	1	0
Definition	MSB of the local IP address							
Default	0x00							

7.5.6.10 PPP Protocol Registers—0x44-0x45

(Read/Write, Default 0xC223)

These registers set the protocol for CPU-generated PPP packets. By default, these registers will be initialized to the CHAP protocol (0xC223). These registers should be set prior to writing any data to the PPP Data Register (0x3C) if a protocol other than CHAP is used.

Table 7-141 PPP Protocol Register Bit Definitions (0x44)

Bit	7	6	5	4	3	2	1	0
Definition	LSB of Protocol							
Default	0x23							

Table 7-142 PPP Protocol Register Bit Definitions (0x45)

Bit	7	6	5	4	3	2	1	0
Definition	MSB of Protocol							
Default	0xC2							

7.5.6.11 CHAP ID Register—0x46

(Read-only, Default N/A)

This register reports the Code-ID from received CHAP Challenge, Ack and Nak packets. It is valid when the CHAP_Dav, CHAP_Ack or CHAP_Nak bits are set in the CHAP Control and Status Register (0x3F).

Table 7-143 CHAP ID Register Bit Definitions (0x46)

Bit	7	6	5	4	3	2	1	0
Definition	CHAP ID Received							
Default	N/A							

7.5.6.12 Peer IP Address Registers—0x48-0x4B

(Read-only, Default 0x00000000)

These registers read the Peer's IP address as resolved in the NCP configuration request packet. These registers are defined in he following tables.

Table 7-144 Peer IP Address Register Bit Definitions (0x48)

Bit	7	6	5	4	3	2	1	0
Definition	LSB of Peer IP Address							
Default	0x00							

Table 7-145 Peer IP Address Register Bit Definitions (0x49)

Bit	7	6	5	4	3	2	1	0
Definition	Third byte of Peer IP Address							
Default	0x00							

Table 7-146 Peer IP Address Register Bit Definitions (0x4A)

Bit	7	6	5	4	3	2	1	0
Definition	Second byte of Peer IP Address							
Default	0x00							

Table 7-147 Peer IP Address Register Bit Definitions (0x4B)

Bit	7	6	5	4	3	2	1	0
Definition	MSB of Peer IP Address							
Default	0x00							

7.5.6.13 PPP Data Length Registers—0x4E-0x4F

(Read-only, Default 0x0000)

These registers query the length of PPP data that the CPU can read. These registers are valid when the Chap_Dav bit is set in the CHAP Control and Status Register (0x3F). The count will not decrement with each CPU read. Writing a 0x00 to the LSB register (0x4E) will transmit any entered CHAP response data.

Table 7-148 PPP Data Length Register Bit Definitions (0x4E)

Bit	7	6	5	4	3	2	1	0
Definition	LSB of Data Length							
Default	0x00							

Table 7-149 PPP Data Length Register Bit Definitions (0x4F)

Bit	7	6	5	4	3	2	1	0
Definition	MSB of Data Length							
Default	0x00							

7.5.6.14 PPP State Register—0x50

(Read-only, Default 0x00)

This register indicates the current state of the PPP's LCP and NCP automatons.

Table 7-150 PPP State Register Bit Definitions

Bit	7	6	5	4	3	2	1	0
Definition	NCP State				LCP State			
Default	0x0				0x0			

Table 7-151 PPP State Register Description

Bit	Bit Name	Access	Description
7:4	NCP State	R	This field indicates the current state of the NCP automaton as defined in the following table.
3:0	LCP State	R	This field indicates the current state of the LCP automaton as defined in the following table.

Table 7-152 NCP and LCP States

State	Definition
0	Initial State
1	Starting State
2	Closed State
3	Stopped State
4	Closing State
5	Stopping State
6	Req-Sent State
7	Ack Received State
8	Ack Sent State
9	Opened State

For more information on each of these states, refer to the PPP RFC.

NOTE: About establishing a PPP connection, always confirm that the PPP_Up/SRst bit in the PPP Control/Status register (0×32) is 1, or that the status code in the PPP Interrupt Code register (0×38) is "0×09."

7.5.6.15 MRU Registers—0x52-0x53

(Read-only, Default 0x05DC)

These registers report back the MRU that the peer requested during the LCP negotiation phase. This value is valid after the LCP has reached State 9. The LCP State can be determined by reading the PPP State Register (0x50).

Table 7-153 MRU Low Register Bit Definitions (0x52)

Bit	7	6	5	4	3	2	1	0
Definition	LSB of MRU							
Default	0xDC							

Table 7-154 MRU High Register Bit Definitions (0x53)

Bit	7	6	5	4	3	2	1	0
Definition	LSB of MRU							
Default	0x05							

7.5.6.16 Serial Port Revision Register—0x71

(Read-only, Default 0x20)

This register reports back the revision ID for the serial port. This value is currently set to 0x20.

Table 7-155 Serial Port Revision Register Bit Definitions

Bit	7	6	5	4	3	2	1	0
Definition	Serial Port Revision							
Default	0	0	1	0	0	0	0	0

7.5.6.17 Serial Port Configuration Register—0x72

(Read/Write, Default 000X0110B)

This register configures the serial port as shown in the following tables.

Table 7-156 Serial Port Configuration Register Bit Definitions

Bit	7	6	5	4	3	2	1	0
Definition	-	-	HWFC	CTS	-	DTR	RTS	SCTL
Default	0	0	0	-	0	1	1	0

NOTE: Reserved bits are signified by a dash (-). All reserved bits should be written as “0”.

Table 7-157 Serial Port Configuration Register Description

Bit	Bit Name	Access	Description
5	HWFC	R/W	Hardware Flow Control When this bit is written it controls the hardware flow control: 0 = Hardware Flow Control is deactivated (default) 1 = Hardware Flow Control activated Refer to the Modem and Serial Port Chapter for more information about Hardware Flow Control.
4	CTS	R	Clear to Send When read, this bit reflects the current state of the CTS signal on the serial port. It is independent of the SCTL bit setting.
2	DTR	R/W	Data Terminal Ready When read, this bit reflects the current state of the DTR bit on the serial port. When written, the CPU controls the state of the DTR bit.
1	RTS	R/W	Request To Send When read, this bit reflects the current state of the RTS bit on the serial port. When written, the CPU can control the state of the RTS bit.
0	SCTL	R/W	Serial Port Control This bit determines if the CPU or the Network Stack controls the serial port. When this bit is low (default), the CPU controls the port. When the bit is high, the Network Stack controls the serial port. 0 = CPU controls port (default) 1 = Network Stack controls port

7.5.6.18 Serial Port Status Register—0x73

(Read-only)

This register provides the external modem status to the Network Stack. This register configures the serial port as shown in the following tables.

Table 7-158 Serial Port Status Register Bit Definitions

Bit	7	6	5	4	3	2	1	0
Definition	Data_Av	DCD	DSR	CTS	RI	DTR	RTS	SCTL
Default	0	-	-	-	-	1	1	0

Table 7-159 Serial Port Status Register Description

Bit	Bit Name	Access	Description
7	Data_Av	R	Serial Data Available When read, this bit indicates that Serial Port data is available. 0 = No data available 1 = Data available
6	DCD	R	Data Carrier Detect This bit reflects the current state of the DCD bit on the serial port.
5	DSR	R	Data Send Ready When read, this bit reflects the current state of the DSR bit on the serial port.
4	CTS	R	Clear to Send This bit reflects the current state of the CTS bit on the serial port.
3	RI	R	Ring Indicator This bit reflects the current state of the RI bit on the serial port.
2	DTR	R	Data Terminal Ready When read, this bit reflects the current state of the DTR bit on the serial port.
1	RTS	R	Request To Send When read, this bit reflects the current state of the RTS bit on the serial port.
0	SCTL	R	Serial Port Control This bit indicates whether the CPU or the Network Stack is controlling the serial port. 0 = CPU controls port (default) 1 = Network Stack controls port

7.5.6.19 Serial Port Interrupt Enable Register—0x76

(Read/Write, Default 0x00)

This register enables the serial port interrupts. The default for this register is 0x00 (interrupts disabled).

Table 7-160 Serial Port Interrupt Enable Register Bit Definitions

Bit	7	6	5	4	3	2	1	0
Definition	PInt_En	DSInt_En	DVInt_En	DCDInt_En	-	-	-	-
Default	0	0	0	0	0	0	0	0

NOTE: Reserved bits are signified by a dash (-). All reserved bits should be written as “0”.

Table 7-161 Serial Port Interrupt Enable Register Description

Bit	Bit Name	Access	Description
7	PInt_En	R/W	Port Interrupt Enable This is the enable for the PInt bit (bit 7, Register 0x78). This is the master enable bit for Serial Port Interrupt.
6	DSInt_En	R/W	Data Sent Interrupt Enable This is the enable for the DSInt bit (bit 6, Register 0x78).
5	DVInt_En	R/W	Data Available Interrupt Enable This is the enable for the DVInt bit (bit 5, Register 0x78).
4	DCDInt_En	R/W	DCD Interrupt Enable This is the enable for the DCDInt factor of PInt bit (bit 7, Register 0x78).

7.5.6.20 Serial Port Interrupt Register—0x78

(Read-only, Default 0x00)

This register indicates the state of the serial port interrupts.

Table 7-162 Serial Port Interrupt Register Bit Definitions

Bit	7	6	5	4	3	2	1	0
Definition	PInt	DSInt	DVInt	DCDInt	-	-	-	-
Default	0	0	0	0	0	0	0	0

NOTE: Reserved bits are signified by a dash (-). All reserved bits should be written as "0".

Table 7-163 Serial Port Interrupt Register Description

Bit	Bit Name	Access	Description
7	PInt	R	Port Interrupt This interrupt triggers when there is data available for the CPU to read or data written by the CPU to the serial port has been sent. Reading all available data or clearing DSInt will clear this interrupt. Also, this interrupt triggers when there is a level change on DCD input pin. Refer to Serial Port Interrupt Enable Register for the enable means.
6	DSInt	R	Data Sent Interrupt This interrupt triggers when all of the available data, written by the CPU to the serial port, has been sent.
5	DVInt	R	Data Available Interrupt This interrupt triggers when data in the serial port is available to be read by the CPU.
4	DCDInt	R/W	DCD Interrupt This interrupt occurs regardless of the state of DCDInt_en bit(bit 4, Register 0x76) when there is a level change on the DCD input pin. This bit clears the interrupt status when a “1” is written to it.

7.5.6.21 Serial Port Data Register—0x7C

(Read/Write, Default 0x0000)

This register sends data to and reads data from the serial port UART. The data is valid when the Data_Av bit in the Serial Port Status Register (bit 7, 0x73) is set. Data can be written to the Serial Port Data Register if the DSInt bit in the Serial Port Interrupt Register (bit 6, 0x78) is set.

Note: This register should only be used when the SCTL bit in the Serial Port Configuration Register (0x72) is low.

7.5.6.22 Serial Port BAUD Rate Divider Registers—0x80-0x81

(Read/Write, Default 0x0000)

These registers set the BAUD rate for the serial port. Calculate the value by using the following formula:

Program Value = [(clk Frequency) / (BAUD Rate)] - 1

Where clk, is the clock rate for the S-7601A.

Example:

When the S-7601A clock rate is 256 kHz and a BAUD rate of 64 Kbps is desired, the programmed value should be:

(256 kHz / 64 k) - 1 = 4 - 1 = 3

Note: The lowest value that should be programmed into these registers is 0x0003.

8 Data Communications

8.1 Serial Port Interface

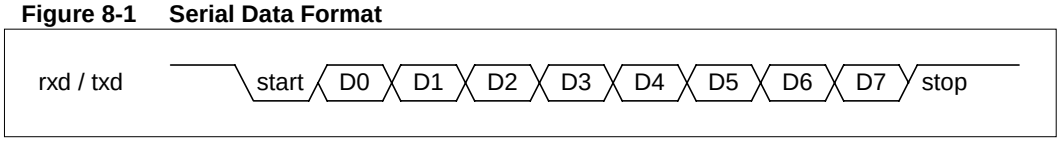
8.1.1 Overview

The Modem port uses the standard 8 bit serial data format., and supports a 16 byte receive FIFO and hardware flow control.. The BAUD rate is set via the BAUD Rate Divide registers.

8.1.2 Data Format

The data format used is 8 data bits, 1 start bit (logic 0), 1 stop bit (logic 1), and no parity. The data is sent lsb first. This format is shown in figure 6-1.

Figure 8-1 Serial Data Format



8.1.3 Hardware Flow Control

Hardware Flow Control is turned off by default. In this mode, data is transmitted independent of the state of the CTS pin. While the CPU is in control of the serial port, it can monitor the state of all the serial port control signals and control when data gets sent or received, either through polling the status bits or interrupts. It can also control the RTS signal by asserting the RTS bit in the *Serial_Port_Config* register. When the network stack controls the serial port, data will be sent out as soon as it is available from the PPP layer. When receiving data, the software in the CPU control mode should read the data out of the 16-byte FIFO fast enough to prevent buffer overflow.

Hardware Flow Control can be turned on by writing a "1" to bit 5 (DSR/HWFC) of the *Serial_Port_Config* register. With the hardware flow control turned on, full RTS/CTS handshaking is supported. When the serial port detects that CTS is de-asserted, it will stop sending data until CTS is reasserted. Any byte output at the time CTS is de-asserted will complete, but no further bytes will be sent until CTS is asserted.

In the other direction, S-7601A will de-assert RTS if the serial port's 16-byte FIFO is half full. This indicates to the machine on the other end of the serial line to stop transmitting data. The RTS bit will reassert when the CPU or network stack has read data out of the Receive FIFO and room becomes available. If the machine communicating with S-7601A over the serial port does not support RTS/CTS handshaking, the Receive FIFO may overflow and data loss may occur.

8.1.4 Serial Port Control *(for the Extended iAPI Register Map)*

The control of the serial port is turned over to the CPU by default and after any reset condition. In this mode, any data written to the *Serial_Port_Data* register will be sent out and all data received will be made available to the CPU via this same register. Prior to using the data register, the CPU should set the *BAUD_Rate_Div* register to the proper setting. An interrupt can be triggered when data is available from the serial port by asserting the PINT_EN bit. When this bit is asserted, an interrupt will trigger any time that there is data available to be read from the port. If there is more then one byte in the Receive FIFO, the interrupt will remain active until all bytes are read. An interrupt can also

be triggered indicating that the outgoing data byte has been sent, by asserting the DSINT_EN bit. This interrupt will trigger whenever there is no more data to be sent.

The CPU turns over control to S-7601A's Network Stack by asserting the SCTL bit in the *Serial_Port_Config* register. When the Network Stack controls the port, the CPU should not access the *Serial_Port_Data* register. The S-7601A chip will automatically send PPP packets to the serial port and read incoming bytes from the serial port. The serial port interrupts are not valid when the Network Stack controls the port.

8.2 TCP/UDP Data Communications (for the Extended iAPI Register Map)

Before a general socket register is accessed, 0x00 (for socket 0) or 0x01 (for socket 1) must be programmed into the Master Index register.
Before a PPP module register is accessed, 0x80 must be programmed into the Master Index register.

8.2.1 TCP Data Communications

Data communication is held with the SCTL-bit in the Serial Port Config register set to "1." For data transmission, data is written to the Socket Data register (0x3C). The S-7601A stores data in its outgoing buffer via the Socket Data register. The address of the outgoing buffer is specified by the Buffer Out Length register (0x4C-0x4D). The value of the Buffer Out Length register becomes 0x03ff when the outgoing buffer is empty. The value of the Buffer Out Length register decrements each time one byte of data is written to the Socket Data register.
After the data has been written, if "1" is written to the Send_Go bit in the Socket Command register (0x3A), data in the outgoing buffer is processed by protocols and transmitted. The value of the Buffer Out Length register increments by the number of bytes of transmitted data. Therefore, the value of the register returns to 0x03ff after all data has been sent.
In data transmission, the outgoing buffer can hold up to 1,023 bytes of data. Datagrams longer than 1,023 bytes must be split by the MPU, and transmitted in chunks. When the outgoing buffer contains 1,023 bytes of data, the value of the Buffer Out Length register becomes 0x0000. No more data must be written to the Socket Data register.
At this point, "1" is written to the Send_Go bit in the Socket Command register, and data in the outgoing buffer is sent. After confirming that all data in the outgoing buffer has been sent, and that the value of the Buffer Out Length register returns to 0x03ff, the MPU sends the remaining datagrams. This procedure is repeated.
Transmission of all data in the outgoing buffer can be confirmed by the Snd_Emp bit in the Socket Status 0 register (0x34). After an interrupt is received, this transmission can also be confirmed by the Snd_Emp bit in the Socket Interrupt Status 0 register (0x38).

When receiving data, the S-7601A applies protocol processing, and stores the data in the incoming buffer.
The address of the incoming buffer is specified by the Buffer In Length register (0x4E-0x4F). The value of the Buffer In Length register is 0x0000 when the incoming buffer is empty. When the incoming buffer contains data, the value of the register increments by the number of bytes of stored data. The Buffer In Length register containing a value other than 0x0000 indicates data reception. The Rcv_Dav bit in the Socket Status 0 register (0x34), or the Socket Data Available register or the Rcv_Dav bit in the Socket Interrupt Status 0 register (0x38) (after an interrupt is received) also indicates data reception.
Reading the Socket Data register (0x3C) while checking the Rcv_Dav bit in the Socket Status 0 register (0x34) obtains data from the incoming buffer.
Each time one byte of data is read from the Socket Data register, the value of the Buffer In Length register decrements. After all data has been read, the value of the register returns to 0x0000.
For TCP data reception, the incoming buffer can hold up to 2,047 bytes of data. The S-7601A and its peer apply TCP protocols to prevent their incoming buffers from overflowing.

8.2.2 UDP Data Communications

In the UDP mode, the procedure of data transmission is the same as in the TCP mode. The application layer is responsible for preventing their incoming buffers from overflowing. In the UDP_Raw mode, when receiving data, the S-7601A applies UDP protocol processing. Then, the S-7601A adds 12 bytes of header information to the data, and stores it in the incoming buffer.
First, 12 bytes of header information is obtained, then data is obtained from the incoming buffer. In this mode, the incoming buffer can hold up to 2,047 bytes of data including 12 bytes of header information.

Table 8-1 shows the structure of header information.

Table 8-1 Structure of header information

Number of bytes from the beginning	Details of bytes	Remarks
0	The most significant byte of the remote IP address	
1	The second byte of the remote IP address	
2	The third byte of the remote IP address	
3	The least significant byte of the remote IP address	
4	The most significant byte of the remote port number	
5	The least significant byte of the remote port number	
6	The most significant byte of the local port number	
7	The least significant byte of the local port number	
8	The most significant byte of the UDP datagram size	Eight bytes of the UDP header are not included.
9	The least significant byte of the UDP datagram size	
10	The most significant byte of the UDP checksum	
11	The least significant byte of the UDP checksum	

9 Reset Functions

9.1 Overview

The S-7601A has the following four reset functions, each of which has a different scope.

9.1.1 Hardware Reset Function

The hardware reset function initializes the entire S-7601A internal circuit.
The S-7601A operates in synchronization with the CLK signal (clock input). If the RESETX pin is set to "L" during a minimum of two clock periods, the S-7601A accepts a hardware reset input, and starts initializing the internal circuit at the rising edge of the fourth clock. After the RESETX pin is pulled "H," the S-7601A remains initialized, and returns to the normal state at the rising edge of the fourth clock. See the Figure 9-1.

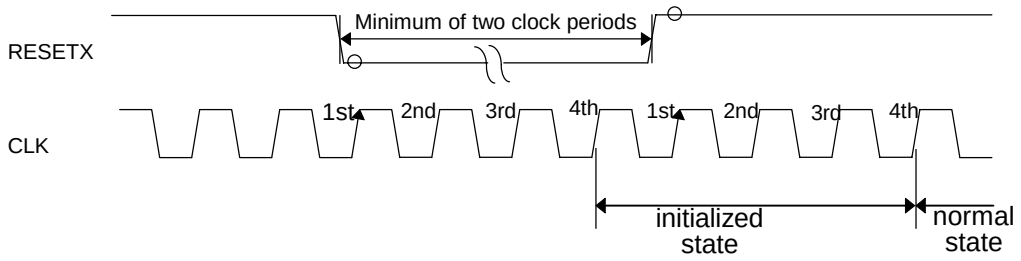


Figure 9-1 Hardware Reset Timing

9.1.2 Software Reset Function

The software reset function initializes the internal circuit excluding the physical layer block. This is done by writing "1" (twice continuously) to the SW_Rst bit in the General Control register (0x01).

S-7600A-compatible mode Register Mapping

Registers of the following address are not initialized.
0x08,0x09,0x0A,0x0B,0x0C,0x0D and PT_INT bit in 0x04
Note: When PT_INT bit continues being "1", interrupt is still active. Initialize the registers by the following procedure before setting up the respective registers.
Serial_Port_Int_Mask < 0x00 (Write 0x00 to Serial_Port_Int_Mask register)
General_Control < 0x01
General_Control < 0x01

Extended registers mode Register Mapping

Registers of the following address are not initialized.
0x72,0x73,0x76,0x78,0x7C,0x80,0x81 when an index register is 0x80, and PT_Int bit in 0x04.
Note: When PT_Int bit continues being "1", interrupt is still active. Initialize the registers by the following procedure before setting up the respective registers.
Master_Index < 0x80 (Write 0x80 to Master_Index (0x20) register)
SP_Int_Enable <0x00
General_Control < 0x01
General_Control < 0x01
General_Control < 0x04
Master_Index < 0x80
SP_Int <0x10

9.1.3 Socket Reset Function

The socket reset function initializes parameters for each general socket.
For the S-7600A-compatible iAPI register map, sockets are initialized by writing "1" to the Data_Avail/RST bit in the Socket Config Status Low register (0x22). Before resetting sockets, make sure that the Snd_Bsy bit in the Socket Status High register (0x3A) is "0."
For the extended iAPI register map, sockets are initialized by writing "1" to the Sck_Clr bit in the Socket Command register (0x3A). Before resetting sockets, make sure that the Sck_Busy bit in the Socket Status register 2 (0x5A) is "0."

9.1.4 PPP Reset Function

The PPP reset function initializes the PPP engine. For the S-7600A-compatible iAPI register map, the PPP engine is initialized by writing "1" to the PPP_UP/SRst bit in the PPP Control Status register (0x60).
For the extended iAPI register map, the PPP engine is initialized by writing "1" to the PPP_UP/Rst bit in the PPP Control and Status register (0x32).

10 Application Examples

10.1 In Case of x80 Family MPU

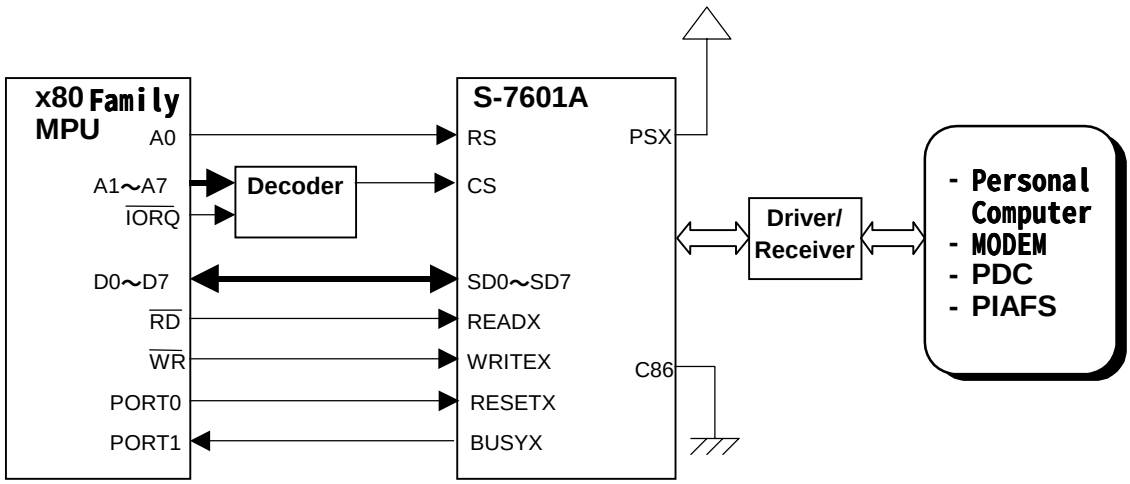


Figure 10-1 Example of x80 Family MPU

10.2 In Case of 68k Family MPU

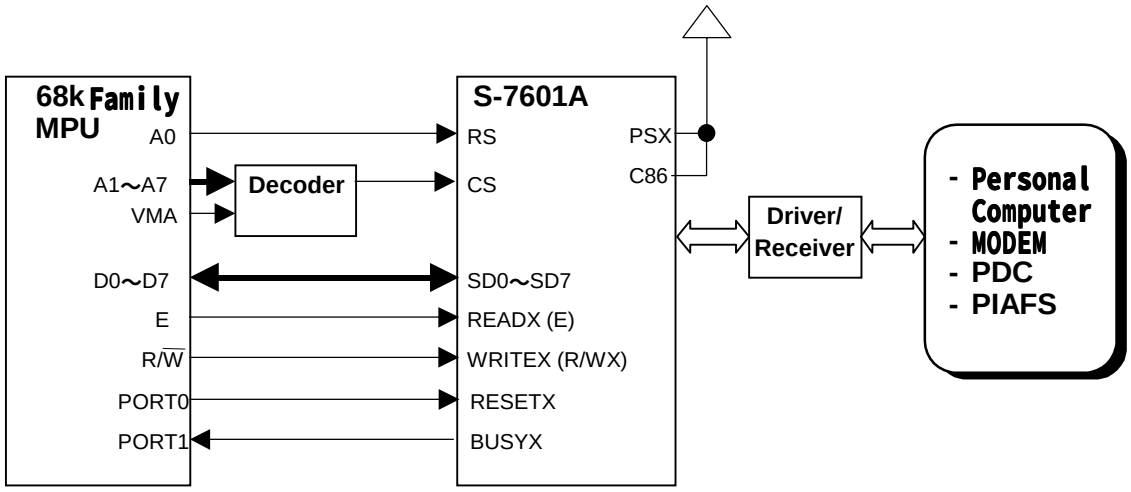


Figure 10-2 Example of 68k Family MPU

10.3 In Case of SII Serial Interface

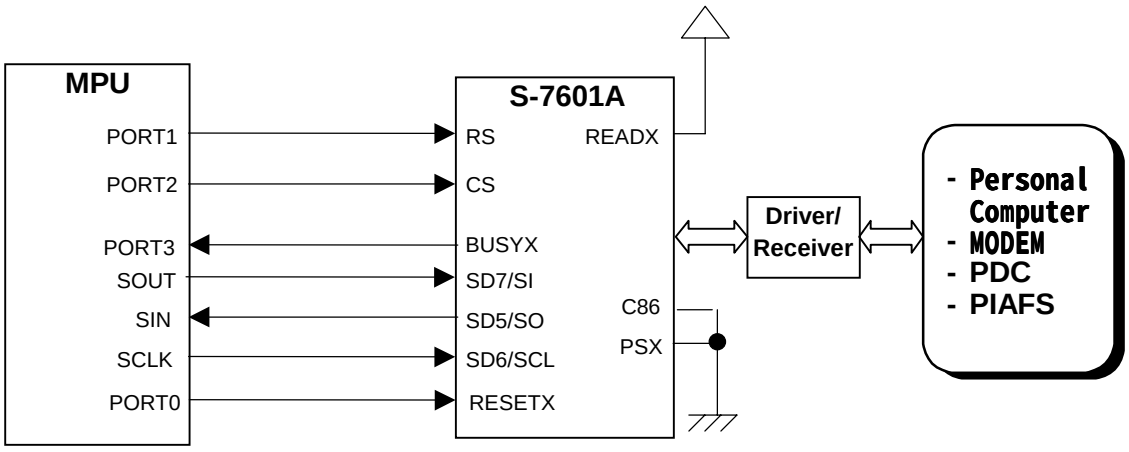


Figure 10-3 Example of SII Serial Interface

10.4 In Case of SPI Serial Interface

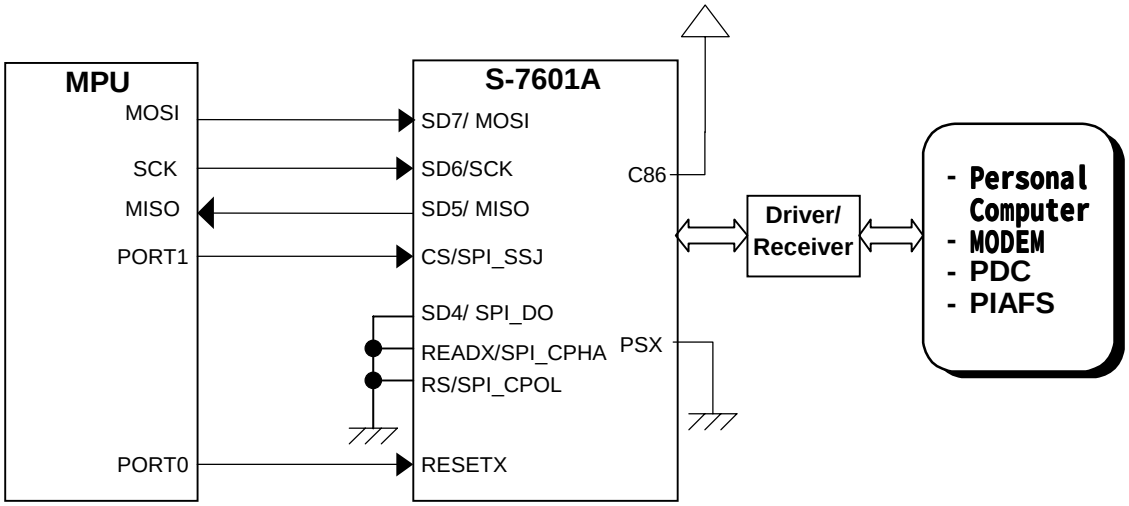


Figure 10-4 Example of SPI Serial Interface

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The S7601A TCP/IP Network Stack LSI is based upon iReady's Internet Tuner® technology.
The URL for iReady's Web site is,
http://www.iready.com

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